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OHMIC CONTACTS TO GALLIUM ALUMINUM ARSENIDE FOR HIGH TEMPERATURE APPLICATIONS

FINAL TECHNICAL REPORT FOR THE PERIOD
July 1, 1985 through February 29, 1988

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Building 410
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R.W. Grant and J.R. Waldrop
Principal Investigators

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A new approach for fabricating nonalloyed ohmic contacts to GaAs was developed. The approach uses ultrathin (15-30Å) layers of heavily doped Ge or Si in contact with GaAs to alter the Schottky barrier height (ϕ_B) at the GaAs interface. For n-type GaAs ϕ_B could be varied from about 0.3 to 1.0 eV. The low barriers are useful for tunneling ohmic contacts to n-GaAs while the high barriers should be useful for p-GaAs ohmic contacts and for FET gate applications. In some instances it was necessary to interpose a thin nonmetallic electrically conducting barrier between the contact metal and the thin Ge or Si layer to preserve optimum contact properties. Specific contact resistivity (ρ_c) measurements indicated that $\rho_c < 10^{-6}$ Ω-cm^2 should be obtainable in practical contacts to heavily doped material. It is generally observed that ϕ_B at most GaAs interfaces is confined to a relatively narrow range presumably

Contact resistivity ≤ 10 to the -6 Ohms/sq.cm

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19. ABSTRACT (Cont'd)

Phi B

due to a large concentration of acceptor and donor states closely spaced in energy near midgap. The new approach for normalized ohmic contact fabrication suggests that these states can be saturated with carriers from the heavily doped Ge or Si so as to substantially modify ϕ_B. The resulting contact ϕ_B is virtually independent of contact metallization; the heterojunction band alignment characteristics at the Ge or Si interface with GaAs determine the ϕ_B of the contact. *(R_W)*

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1.0 INTRODUCTION

This is the final report for Contract No. F49620-85-C-0120 entitled, "Ohmic Contacts to Gallium Aluminum Arsenide for High Temperature Applications," for the period 07/01/85 through 02/29/88. The material properties of GaAs (e.g., high electron mobility, radiation hardness and ease of heterojunction fabrication) make it an attractive semiconductor for use in advanced DoD systems applications that require high frequency operation and high data processing rates. New types of heterostructure devices are being developed in the rapidly progressing area of GaAs IC technology. These heterostructure devices include the GaAs heterojunction bipolar transistor (HBT) for which remarkable current gain cutoff frequencies above 120 GHz have been reported.[1] Increased circuit complexity and high-frequency operation require decreased device dimensons. This size reduction puts greater importance on ohmic contact quality, especially with regard to spatial uniformity of electrical properties and surface morphology. Nonideal ohmic contacts can limit frequency response and nonuniform contacts can affect the yield of ICs.

Although GaAs IC technology has developed rapidly, the rather empirical nature of ohmic contact metallurgy indicates that the basic contact formation mechanism is not well understood.[2] Improved ohmic contacts to both n- and p-type $Ga_{1-x}Al_xAs$ material are needed. The most widely used ohmic contact to n- GaAs is the alloyed AuGeNi metallization.[3] Several studies have shown that these alloyed contacts have multiphase structures with the phase size and composition being dependent on alloying conditions.[4-7] The alloying process involves melting and resolidification of material on a $10^3 Å$ scale. Consequently, alloying requires careful control to achieve reproducibility. It appears that alloyed ohmic contacts are not fully adaptable for small dimension device applications and that to obtain contacts with better uniformity, reproducibility, and reliability nonalloyed contacts need to be developed.

The development of stable nonalloyed ohmic contacts to $Ga_{1-x}Al_xAs$ is of considerable technological importance and could benefit several GaAs device structures. As an example, the Rockwell HBT development effort uses a material structure that consists of several thin layers of $Ga_{1-x}Al_xAs$ or related materials to

achieve high speed response.[1] To optimize HBT performance, parasitic resistances and capacitances must be minimized. The emitter contact resistance is a key parameter; typically, an emitter specific contact resistance of $\leq 5 \times 10^{-7}$ $\Omega\text{-cm}^2$ is required for high performance HBT operation. The base contact is also critical to HBT performance. Heavily doped p-layers are necessary to minimize base resistance and very thin layers are used to optimize current gain. It is important not to alloy the p-type ohmic contact through the base layer during processing. As GaAs device dimensions decrease to improve performance, self-aligned processing techniques based on ion implantation become increasingly important. A self-aligned structure places severe constraints on contact properties if the contact metallurgy is required to withstand the annealing conditions necessary to activate the ion-implanted dopants used in self-aligned processing. The above considerations emphasize the need to develop nonalloyed ohmic contacts to $Ga_{1-x}Al_xAs$ that have good thermal stability.

Tunneling across a thin barrier region is the most common method of forming an ohmic contact. For n-type GaAs, it is generally observed that metal contacts exhibit Schottky barrier heights (ϕ_B) in the fairly narrow range of 0.7-0.9 eV. By maximizing the dopant concentration at the semiconductor interface, the barrier width is reduced and the contact resistance is minimized. For the commonly used AuGeNi ohmic contact metallization, it is usually assumed that a sizeable Schottky barrier exists at the n-type GaAs interface and that tunneling occurs because of heavy Ge doping of the GaAs near-interface region.[2,8] The tunneling contact model[9] has $\rho_c \sim \exp(C\phi_B N_D^{-1/2})$, where ρ_c is the specific contact resistance, N_D is the net donor concentration, and C is a constant. For n-GaAs, a maximum N_D limit of $\sim 5 \times 10^{19}$ cm^{-3} (Sn) has been reported.[10] For this N_D and a $\phi_B = 0.7$ eV, one can estimate a lower limit of $\sim 1.5 \times 10^{-6}$ $\Omega\text{-cm}^2$ for ρ_c.[11] Consistent with this limit are specific contact resistances of $\sim 1 \times 10^{-6}$ $\Omega\text{-cm}^2$ for the AuGeNi metallization[4] and of low 10^{-6} $\Omega\text{-cm}^2$ for Ge/Mo sintered contacts[12] (i.e., contacts in which a thin layer of dopant at the GaAs interface is capped with a high melting point metal). As mentioned above, this lower limit is not acceptable for some GaAs heterostructure device applications.

If the barrier height at a tunneling contact could be reduced, a substantial reduction in ρ_c could be achieved because ρ_c depends exponentially on ϕ_B. Although the

barrier height of most n-type GaAs interfaces is confined to the fairly narrow limits indicated above, there is growing evidence that at some n-GaAs interfaces, much smaller barriers can be obtained.[12-17] Some of these small barrier interfaces are unstable and would not be suitable for contact applications. A major objective of the present program was to develop methods of producing low barrier tunneling contacts to GaAs. The very stable oxides and hydroxides of Al can complicate attainment of good ohmic contacts to $Ga_{1-x}Al_xAs$. This difficulty is often circumvented by making contact to n^+ or p^+ GaAs layers grown on $Ga_{1-x}Al_xAs$ and thus, this program focused on making low barrier contacts to the end member GaAs.

A promising new approach for nonalloyed ohmic contact development was discovered in this program based on the use of ultrathin heterojunction layers (UTHL). Low barrier height contacts to n-GaAs were achieved by using thin (15-30Å) layers of heavily n-type doped Ge and Si. With appropriate diffusion barriers, these low barrier contacts could be preserved in practical contacts. The low barrier nature of the contact was determined by both x-ray photoemission (XPS) and electrical (I-V and C-V) measurements and a model based on the heterojunction characteristics of the contact is proposed to explain the results. The UTHL contact has a barrier height that is virtually independent of the contact metallization. Specific contact resistivity was determined by transmission line measurements (TLM) for a model contact with $N_D = 2 \times 10^{18}$ cm^{-3}. Extrapolation of this result to a contact with $N_D = 5 \times 10^{19}$ cm^{-3} indicated that $\rho_c \sim 2 \times 10^{-7}$ Ω-cm^2 should be obtained. The UTHL approach to ohmic formation should be applicable for p-type ohmic contact formation. A low barrier p-type contact should correspond to a high barrier n-type contact. By using thin (15-30Å) layers of heavily p-type doped Si on n-type GaAs, Schottky barriers of 1 eV were observed which demonstrate the generality of the UTHL method for modifying contact barriers and is consistent with the proposed heterojunction model of contact formation.

The UTHL method for GaAs barrier modification was demonstrated for both Ge and Si interface layers with both n-type (As and P) and p-type (Ga and B) dopants. The associated model offers a means to design a stable high temperature low barrier tunneling ohmic contact by using materials expected to be thermodynamically stable under the annealing conditions used in self-aligned processing.

This report is organized into seven sections. Section 2 discusses the experimental approach used to characterize the GaAs contacts. The materials used in the program are documented in Section 3. In Section 4, the results of XPS interface potential measurements for the Ge and Si overlayers are discussed and related to the heterojunction characteristics of the samples; electrical measurements of corresponding thick contacts obtained by I-V, C-V and TLM are also given. The program is summarized in Section 5 and references are provided in Section 6. The Appendix (Section 7) reproduces four journal publications, three conference talk abstracts and two patent disclosures based on work supported by this program.

2.0 EXPERIMENTAL APPROACH

The XPS system in which the GaAs contacts were prepared and analyzed is discussed in this section. In addition, the current-voltage (I-V), capacitance-voltage (C-V) and transmission line measurement (TLM) apparatus used for electrical characterization of GaAs contacts is described.

2.1 XPS

A Hewlett-Packard 5950 electron spectrometer was used for the XPS investigations of interface chemistry and potential in this program. A photograph of the instrument is shown in Fig. 1. The spectrometer utilizes a monochromatic AlKα ($h\nu$ = 1486.6 eV) x-ray source to excite photoelectrons. A custom sample preparation chamber is attached to the spectrometer to provide various in-situ specimen treatments. These treatments include sample heating, material deposition and low energy electron diffraction (LEED) analysis. Both the XPS spectrometer and sample preparation chamber operate at UHV with a base pressure of ~ 10^{-10} Torr.

The deposition sources for Ge and most metals were resistively heated W wire baskets. A W wire basket was also used for initial Si depositions although an enclosed Ta wire basket was subsequently found to improve source stability. The As_4 and Te sources were small quartz ovens, the P_2 source was an InP crystal heated by a W wire while avoiding direct line of sight between source and sample and elemental B was included in the Si source to deposit boron-doped silicon, Si(B).

The ability of XPS to determine interface chemistry by analyzing chemical shifts is well known.[18] The technique also provides a method to determine the interface Fermi level (E_F^i) of a sample.[19] The determination of E_F^i is illustrated in Fig. 2, which shows a schematic GaAs band diagram. In this figure, all binding energies (E_B) are referred to the Fermi level (E_F). The conduction band minimum is E_c^{GaAs}, the valence band maximum is E_v^{GaAs}, the Ga3d and As3d core level binding energies are E_{Ga3d}^{GaAs} and E_{As3d}^{GaAs}, respectively. E_F^i is measured relative to E_v^{GaAs} at the interface and W is the depletion width. The typical electron escape depth (~ 25Å)[20] is much shorter than W for moderately doped GaAs. For our experimental geometry, the effective photoelectron

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Fig. 1 Photograph of XPS apparatus.

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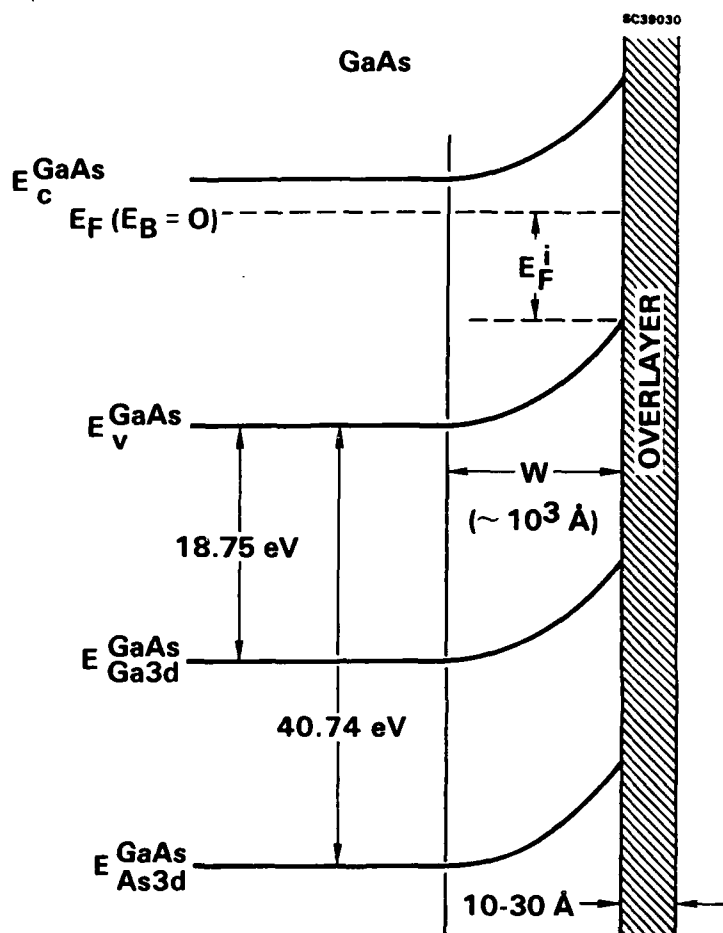
Fig. 2 Schematic band diagram that illustrates the use of XPS to determine E_F^i .

escape depth was always ~ 16Å. Thus, an XPS measurement of a clean GaAs surface or a surface with a very thin overlayer ($\leq$ 25Å) will determine E_{Ga3d}^{GaAs} and/or E_{As3d}^{GaAs} at the interface, as shown in Fig. 2. For GaAs, the binding energy differences

$E_{Ga3d}^{GaAs} - E_v^{GaAs} = 18.75 \pm 0.03$ eV and $E_{As3d}^{GaAs} - E_v^{GaAs} = 40.74 \pm 0.03$ eV have been determined previously.[21] As can be seen in Fig. 2, the interface potential is determined as $E_F^i = E_{Ga3d}^{GaAs} - 18.75$ eV $= E_{As3d}^{GaAs} - 40.74$ eV and $\phi_B = 1.43$ eV $- E_F^i$.

To determine the absolute E_B of either the Ga3d or As3d core levels, a background function proportional to the integrated photoelectron intensity was first subtracted from the XPS spectrum in the vicinity of the core level peak. The resulting peak was least-squares fit to a third order polynomial near the peak maximum and near the half height on both sides of the peak to determine the peak center (position of the half width point at half height) and the peak width, Γ (the full width at half height). A representative example of this analysis for a Ga3d peak is shown in Fig. 3. At the conclusion of most experiments, a thick $(> 10^3 \text{Å})$ Au metal layer was evaporated onto the sample surface and an absolute E_F^i value was obtained by indexing the Au4f$_{7/2}$ XPS peak position to 84.00 eV.[22]

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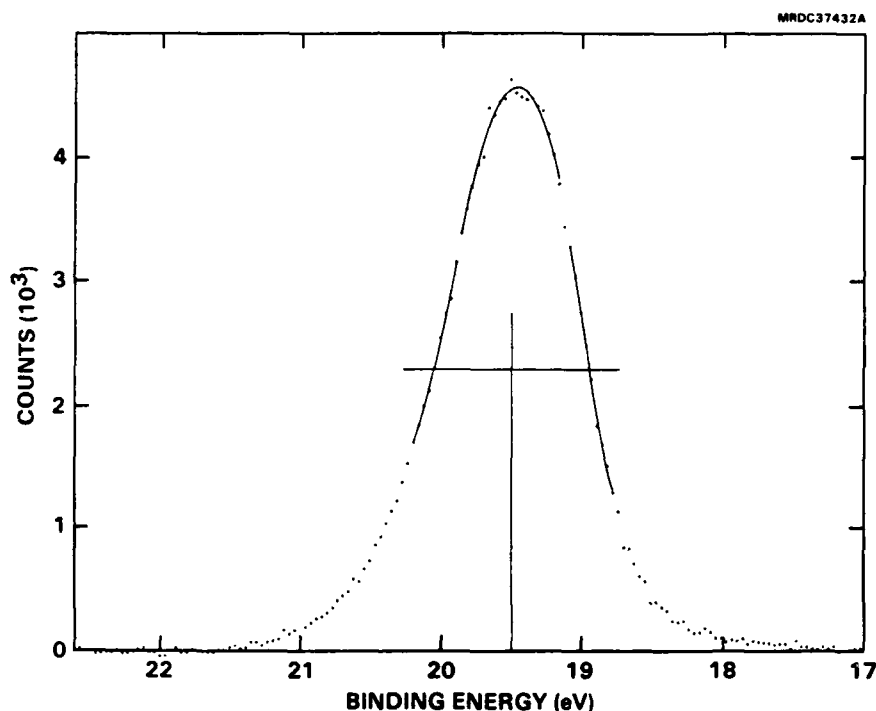
Fig. 3   Analysis method of Ga3d peak used to determine E_F^i from XPS data. Curves are least-square fits to third order polynomials; the peak center and full width at half maximum are indicated.

2.2   I-V and C-V Measurements

The electrical properties of GaAs contacts were characterized by I-V and C-V measurements. I-V data are obtained in 0.01 V forward bias increments by using a computerized system that includes a HP4140B pA meter/voltage source. Both room temperature and low temperature measurements were performed. The low temperature cold stage uses a nitrogen gas Joule-Thomson expansion system. Low temperature measurements were necessary to analyze the low ϕ_B samples. The I-V data were anlayzed by use of the Schottky barrier thermionic emission model with

$$I = I_s exp(qV/nkT) [1 - exp(-qV/kT)]A$$

where both the ideality factor n(at T = 295K, n~ 1.02 is ideal; however there is often an increase in n at low T) and I_s (the saturation current) were determined by a least-squares fit. The ϕ_B was extracted from I_s by

$$I_s = SA* \ T^2 \ exp[-q(\phi_B - \Delta\phi)/kT]A$$

where S is the contact area, A* = 8.16 is the effective Richardson constant, and $\Delta\phi$ is the calculated image force correction ($\Delta\phi$ ±0.04 eV for $\phi_B \geq 0.7$ eV and +0.03 eV for $\phi_B < 0.7$ eV). Good reproducibility of results between contacts on a given sample was observed and thus average values (approximately seven contacts per sample) of ϕ_B and n were determined; the measurement uncertainty for ϕ_B was < ±0.01 eV.

The C-V measurements employed a HP 4275A LCR meter operating at 1 MHz. The C-V data were analyzed according to the conventional model[23] that gives ϕ_B^{CV} in terms of the intercept V_i (found by a least-squares fit) on the voltage axis of a C^{-2} vs V plot.

The interface potential determined by XPS could be compared with corresponding barrier heights determined by I-V or C-V by making measurements on the same sample. First, E_F^1 was determined for a thin (~ 25Å) overlayer; following this determination, a thicker ($\geq 10^3$Å) metallization was deposited in situ. After removal from the ultrahigh vacuum (UHV) system, circular dots were fabricated by chemically

etching a photoresist pattern. In this way, both electrical measurements and XPS measurements could be obtained on the same interface.

2.3   TLM

The specific contact resistance (ρ_c) was measured by the transmission line method (TLM).[24] The contacts were formed on an MBE-grown GaAs layer on a semi-insulating GaAs substrate. A schematic of the test structure is shown in Fig. 4. Two contact masks were fabricated, one to provide test patterns, as shown in Fig. 4(a), and one to facilitate a mesa etch for isolating each test pattern, Fig. 4(b). The rectangular mesa etch mask had dimensions +1 μm larger than the test pattern. A constant current was passed between the large rectangular end contact pads of the test pattern and the subsequent voltage drop between neighboring contact pads was measured. The transmission line model gives the measured resistance as

$$R = R_s \frac{L}{w} + \frac{2L_T}{w} R_s \coth \frac{z}{L_T}$$

where R_s is the sheet resistance, L is the separation between contact pads, w is the contact pad width, L_T is the transfer length, and z is the contact length. When $z \gg L_T$, that is, if the portion of the contact length from which current is flowing is small compared to the total contact length (which is the condition in our measurements), the TLM model reduces to:

$$R = \frac{R_s}{w} L + 2L_T \frac{R_s}{w} .$$

In practice, a plot of R vs L is made from which the slope of a linear least square fit yields $\frac{R_s}{w}$ and the intercept on the L axis for R = 0 yields $2L_T$. The transfer length is related to the contact resistance ρ_c by:

$$\rho_c = R_s L_T^2 .$$

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7.5   10   15   30   45   60   75

(a)

(b)
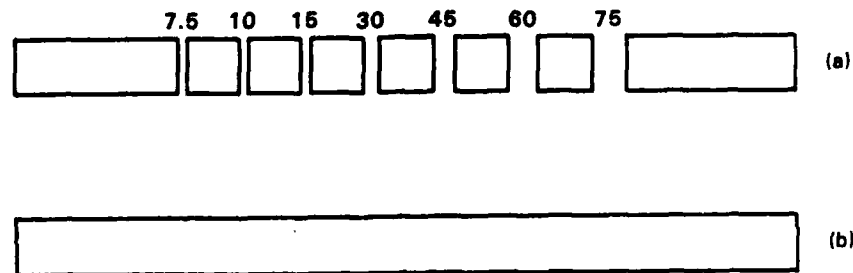
Fig. 4   TLM measurement test pattern. (a) Spacings between squares (in μm) are indicated; square dimensions were 125 × 125 μm, rectangle dimensions were 375 × 125 μm. (b) Rectangular mesa isolation pattern-dimensions 1743.5 × 126 μm.

3.0 MATERIALS

Most of the GaAs material used in this program was bulk grown, (100) oriented, and doped in the $3\text{-}5 \times 10^{16}\,cm^{-3}$ range with either Se or Si. This moderately doped material was utilized so that barrier heights determined by I-V could be analyzed by the thermionic emission model and XPS measurements were not complicated by excessive band bending in the interface region. The material was either grown by the liquid encapsulated Czochralski or horizontal Bridgman techniques. The wafers were obtained in cut and polished form with a 20 mil thickness.

A few GaAs samples were prepared by molecular beam epitaxy at Rockwell for use in TLM measurements. These samples consisted of a 5000Å semi-insulating buffer layer and a 1500Å n-type GaAs layer grown on a semi-insulating GaAs substrate. Net donor densities ranged from 3×10^{17} to $2.3 \times 10^{18}\,cm^{-3}$, as determined by Hall effect measurements.

To prepare a bulk sample for XPS analysis, the GaAs wafer was cut into an approximate 8 × 8 mm square, etched in fresh 4:1:1 H_2SO_4:H_2O_2:H_2O solution for ~ 30 s to remove polishing damage, mounted with indium on a Mo plate and immediately placed into the UHV environment of the XPS system. The In mounting involved heating in air to ~ 160°C for a few seconds. The ~ 10Å native oxide layer was removed by momentary heating, either in vacuum or in an As_4 overpressure, to the minimum necessary temperature (~ 550°C); this heating also forms an ohmic contact between the bulk GaAs and the Mo plate. The thermally cleaned surface is ordered (displays a characteristic LEED pattern) and is shown by XPS to be free of oxygen, carbon, or other contaminants. Following XPS analysis and deposition of thick ($> 10^3$Å) overlayers, circular 2.54×10^{-2} cm diameter dots (for contact electrical characterization) were defined by using photolithography and chemical etching.

The MBE samples used for TLM measurements were prepared in a similar manner except the initial surface was only degreased and not chemically etched. Following contact metallization deposition, the TLM test patterns and isolating mesas were defined by ion milling.

4.0 RESULTS

A new approach for fabricating nonalloyed ohmic contacts is described in this section. The approach uses heavily doped UTHL to alter E_F^i in GaAs. The results for UTHL ohmic contacts formed with either Ge or Si interlayers are presented.

4.1 Ge Overlayers

As noted in Section 1.0, there is growing evidence that at some GaAs interfaces, E_F^i values outside the commonly observed narrow pinning range can be obtained. Specifically relevant to this section is the wide range of E_F^i values reported for the Ge/GaAs interface.[14,15,24-27] If either large E_F^i values could be obtained for n-type contacts or small E_F^i values for p-type contacts, substantial lowering of ρ_c for tunneling contacts could be expected. In Section 4.1.1, we present XPS measurements which show the wide range of E_F^i values obtainable with thin Ge overlayers. The most commonly used ohmic contact to n-type GaAs is the AuGeNi metallization. In Section 4.1.2, we discuss investigations of nonalloyed layer structures of Au, Ge, and Ni which establish a correlation of interface composition and E_F^i. Section 4.1.3 describes TLM measurements of a model UTHL contact which are used to predict expected ρ_c for various N_D.

4.1.1 E_F^i Measurements

The variation in E_F^i for thin overlayers of Ge on n-GaAs can be easily detected by XPS. Representative XPS Ga3d core-level spectra for several samples are compared in Fig. 5. A spectrum from a thermally cleaned surface is shown for reference in Fig. 5(a) (the vertical line shown in the figure marks the center of this Ga3d line). The two spectra shown in Figs. 5(b) and 5(c) are for GaAs samples on which thin layers of Ge were deposited in vacuum at 325 and 250°C, respectively. A LEED pattern was observed for the Ge layers deposited (either in vacuum or in the presence of an As_4 background pressure) in the 200-325°C temperature range, although the pattern had a high background at 200°C. The Ga3d binding energy decrease noted in Figs. 5(b) and 5(c) spectra relative to the thermally clean surface represents a decrease in E_F^i, and thus a corresponding increased band bending. The spectrum shown in Fig. 5(d) is for the same
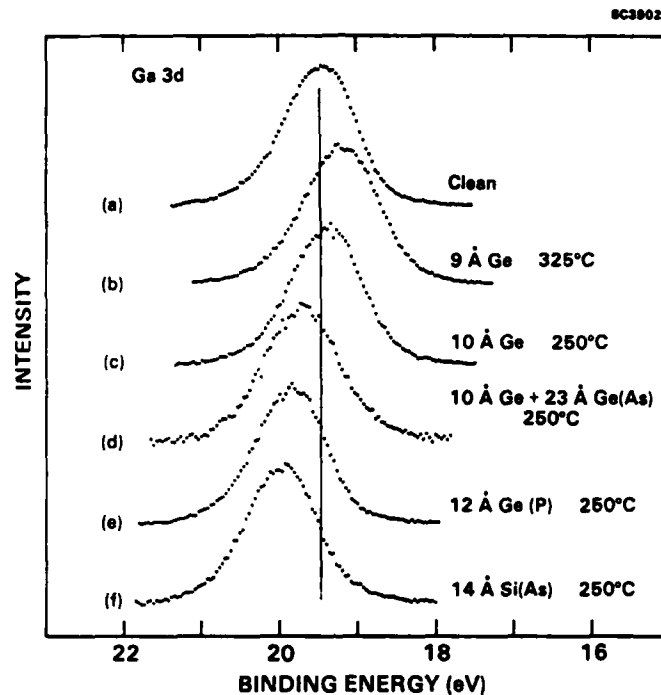
Fig. 5   XPS Ga3d core-level spectra for several GaAs(100) samples with
         thin overlayers. The overlayer composition and deposition
         temperatures are noted in the figure. The spectra shown as
         (c) and (d) are for the same sample, except for the additional
         Ge(As) layer.

sample that was studied in Fig. 5(c), but with the addition of a 23Å-thick layer of Ge
deposited at 250°C under conditions $(1 \times 10^{-7}$ Torr As_4 background pressure) where As
incorporation occurs [this layer is designated Ge(As)]. A marked shift to higher E_B
(lower band bending) occurs.

Two additional spectra are shown in Figs. 5(e) and 5(f). The first is from a
sample on which a 12Å Ge layer was deposited at 250°C in the presence of a 10^{-6} Torr P_2
background. This sample has a substantially lower band-bending than the thermally
cleaned surface. Figure 5(f) is a spectrum from a sample on which a 14Å layer of Si was
deposited at 250°C; these data will be discussed in Section 4.2.1. Values of E_{Ga3d}^{GaAs} and of

the corresponding E_F^i are given in Table 1 for the representative samples shown in Figs. 5(a-e) and for several other samples.

Table 1
Values of E_{Ga3d}^{GaAs} and E_F^i for Several n-GaAs (100) Interfaces

Sample No.	Overlayer	Deposition Temp. (°C)	Overlayer Thickness (Å)	Background Pressure during Deposition (Torr)	E_{Ga3d}^{GaAs} (eV)	E_F^i (eV)
1	Thermally clean (ave. of 16 samples)	---	---	---	19.46	0.71
2	Ge[a]	200	9	Vacuum	19.45	0.70
3	Ge[a]	200	10	Vacuum	19.87	1.12
4	Ge	250	10	Vacuum	19.40	0.65
5	Sample No. 4 + Ge(As)	250	23	10^{-7} As$_4$	19.73	0.98
6	Ge	250	6	Vacuum	19.47	0.72
7	Sample No. 6 + Ge(As)	250	6	10^{-7} As$_4$	19.88	1.13
8	Ge	325	9	Vacuum	19.20	0.45
9	Sample No. 8 + Exposure to 30 L As$_4$ at 325°C	---	---	---	19.26	0.51
10	Ge(As)	RT	26	10^{-7} As$_4$	19.49	0.74
11	Ge(As)	200	10	10^{-7} As$_4$	19.82	1.07
12	Ge(As)	200	7	10^{-7} As$_4$	19.79	1.04
13	Ge(As)[b]	200	9	10^{-7} As$_4$	19.78	1.03
14	Ge(As)	200	11	10^{-7} As$_4$	19.78	1.03
15	Ge(As)[a]	200	4	10^{-7} As$_4$	19.78	1.03
16	Ge(As)	250	9	10^{-7} As$_4$	19.96	1.21
17	Ge(As)	250	9	10^{-7} As$_4$	19.90	1.15
18	Ge(As)	250	8	10^{-7} As$_4$	19.78	1.03
19	Ge(As)	250	7	10^{-7} As$_4$	19.89	1.14
20	Ge(As)	325	11	10^{-7} As$_4$	19.85	1.10
21	Ge(As)	325	9	10^{-6} As$_4$	19.96	1.21
22	Ge(P)	250	11	10^{-6} P$_2$	19.87	1.12

a Substrate cleaned in 10^{-6} Torr As$_4$.
b Substrate cleaned in 10^{-7} Torr As$_4$.

Several of the results listed in Table 1 are shown pictorially in Fig. 6. The overlayer characteristics are noted at the bottom of the figure, and the corresponding E_F^i value is shown on the vertical scale. The positions of E_v^{GaAs} and E_c^{GaAs} are listed on the vertical scale ($E_F^i = 0$ at E_v^{GaAs}) . As will be noted below, the interface heterojunction band alignment characteristics appear to play a role in determining the
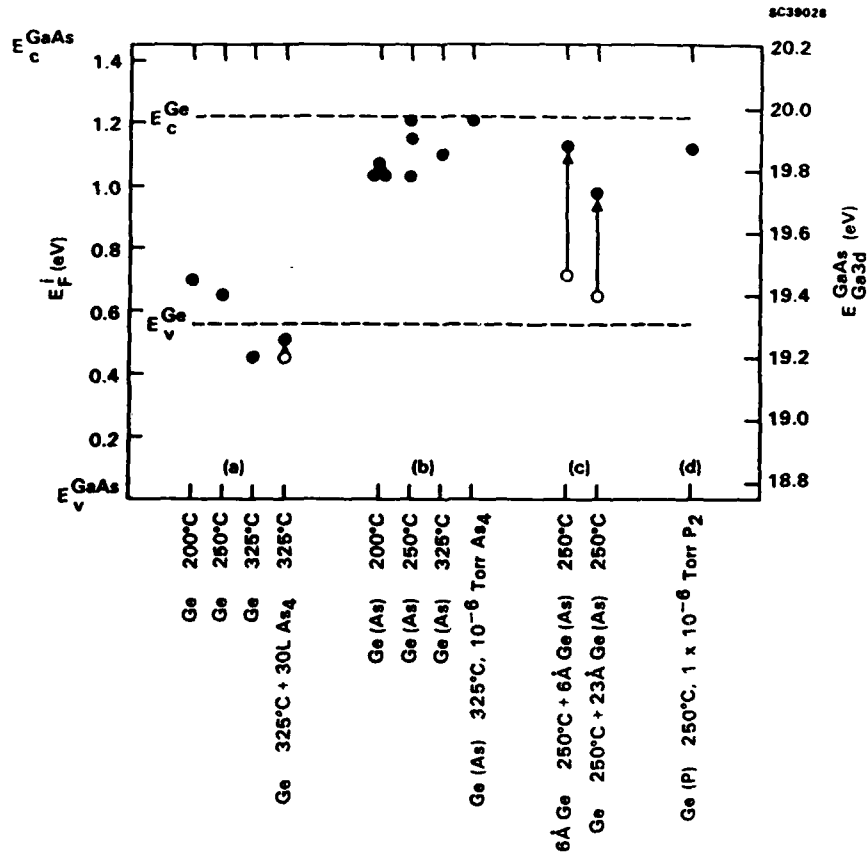
Fig. 6   Summary of several E_F^i measurements. Germanium overlayer charac-
teristics are given at bottom of figure. Unless noted otherwise, over-
layer thicknesses are nominally ~ 10Å and depositions intended to
incorporate As or P in the overlayer were carried out in 10^{-7} Torr
background pressure of As_4 or P_2: (a) overlayers deposited in vacuum;
(b) overlayers deposited in As_4; (c) overlayers initially deposited
in vacuum, but completed with deposition in As_4; (d) overlayer deposited
in P_2.

observed E_F^i positions. Thus, also shown in this figure by dashed lines are the E_v and E_c
positions for Ge measured at Ge/GaAs[28] heterojunction interfaces.

The data shown in Fig. 6 are grouped into four sets (a)–(d). The first set (a) shows E_F^i values obtained with Ge overlayers that were deposited in vacuum between 200 and 325°C. The data indicate that band bending in the GaAs increases slightly with increasing Ge deposition temperature. Vacuum-deposited Ge is almost always found to be p-type,[29] independent of the substrate. The results shown in Fig. 6(a) suggest that the acceptor density (asociated with either the deposition process and/or Ga incorporation from the substrate) increases with increasing deposition temperature. The Ge is degenerate p-type when vacuum deposited at 325°C on thermally cleaned GaAs substrates, in agreement with previous results.[25] Exposure of the Ge overlayer grown at 325°C to 30 L of As_4 with the sample held at 325°C caused only a small (~ 0.06 eV) decrease in GaAs band bending, as indicated by the arrow in Fig. 6(a).

The E_F^i values shown in Fig. 6(b) are for Ge(As) overlayers deposited between 200 and 325°C. The net donor density associated with As-doped, molecular beam epitaxy (MBE)-grown Ge films on GaAs (100) has been studied[11,30] as a function of substrate temperature and found to vary relatively slowly in this temperature range. This behavior may be related to the relatively small variation of E_F^i with substrate temperature observed in Fig. 6(b), where there is a tendency for E_F^i to increase with increasing substrate temperature and with increasing As_4 background pressure during Ge deposition. The observed E_F^i values are in the same range as those previously observed for n-Ge layers grown on several GaAs(100) surfaces,[15] and support the conclusion that As doping of Ge is important in determining E_F^i while deposition-induced defects are not.[26]

To investigate the role of As in determining E_F^i, two additional experiments were performed in an effort to separate the effect of As at the Ge/GaAs interface from As incorporated in the Ge overlayer. The results of these two experiments are shown in Fig. 6(c). In this case, the sample has two overlayers. The first layer was Ge deposited in vacuum at 250°C; the E_F^i value associated with this layer is shown by the open circles. The second Ge(As) overlayer was deposited at 250°C in the presence of 10^{-7} Torr As_4 background pressure. The E_F^i observed after deposition of the Ge(As) layer is shown by closed circles. The large increase in the E_F^i position (decrease in GaAs band bending) is indicated by arrows in Fig. 6(c). In Fig. 6(a), it was observed that exposure of

a vacuum-deposited Ge layer to As_4 caused only a minor shift of $E_F^{\dagger}$. Taken together with the results shown in Fig. 6(c), it appears that the role of As is to alter the E_F in the deposited Ge and thus the Ge/GaAs $E_F^{\dagger}$ rather than directly affecting the interface properties per se.

If As acting as a donor in Ge is responsible for the large $E_F^{\dagger}$ values, other n-type dopants might be expected to produce a similar effect. Thus, a Ge(P) overlayer was prepared by depositing Ge at 250°C in a 10^{-6} Torr P_2 background pressure. The measured $E_F^{\dagger}$ value is shown in Fig. 6(d) and is similar to the results obtained with Ge(As) layers.

The above noted range in $E_F^{\dagger}$ indicates that interface heterojunction band alignment characteristics may be responsible for the limits to the large range of observed $E_F^{\dagger}$ values at the Ge/GaAs interface. This possibility will be further discussed in Section 4.2.1.

4.1.2   Model AuGeNi Contacts

The alloyed AuGeNi metallization[3] is widely used as an ohmic contact to n-GaAs. The complex contact structure consists of several phases whose individual size and composition depend on the alloying time and temperature.[7,31-33] It is usually assumed that ϕ_B is inevitably ~ 0.7-0.9 eV because, as noted previously, the Schottky barrier height for most metal contacts to GaAs is in this range. According to this viewpoint, ρ_c is reduced by minimizing N_D. However, as observed in Section 4.1.1, for certain thin Ge overlayers on clean GaAs, $E_F^{\dagger}$ can be > 1.0 eV. If such a high $E_F^{\dagger}$ state (low ϕ_B) can be attained in a tunnel AuGeNi ohmic contact, ρ_c would be substantially reduced for a given N_D.

An investigation of model AuGeNi contacts to GaAs was carried out that involved layered structures designed to correlate interface composition with ϕ_B. The contacts were not alloyed so as to retain interfaces of controlled composition. The interface chemistry and $E_F^{\dagger}$ during initial contact formation were observed by XPS; the corresponding ϕ_B for a thick contact was obtained by I-V measurement.

The contact interfaces were prepared under UHV conditions in the sample preparation chamber of the XPS system. During initial contact formation, XPS spectra of the Ga3d and As3d core level peaks in GaAs and of other core level peak spectra appropriate for a given interface were obtained. The $NiAs_x$ layers were formed by depositing Ni onto a room temperature substrate in a 10^{-7}-10^{-6} Torr As_4 overpressure (XPS analysis indicated that the $NiAs_x$ layers were As rich).

The respresentative Ga3d core level peak data plotted in Fig. 7 show how XPS was used to measure E_F^1 and to monitor composition during interface formation. The upper three spectra are after sequential treatments to the same sample; the lower three are for three other samples with the indicated overlayer structure (peak heights are normalized). The vertical line in Fig. 7 that marks the center of the clean surface Ga3d peak at 19.47 eV is for E_F^1 (clean) = 0.67 eV.

SC36451

Ga 3d

INTENSITY

clean

9Å Ge(As)

9Å NiAs$_x$-9Å Ge(As)

11Å Te-10Å Ge(As)

7Å Au-8Å Ge(As)

18Å Ni-10Å Ge(As)

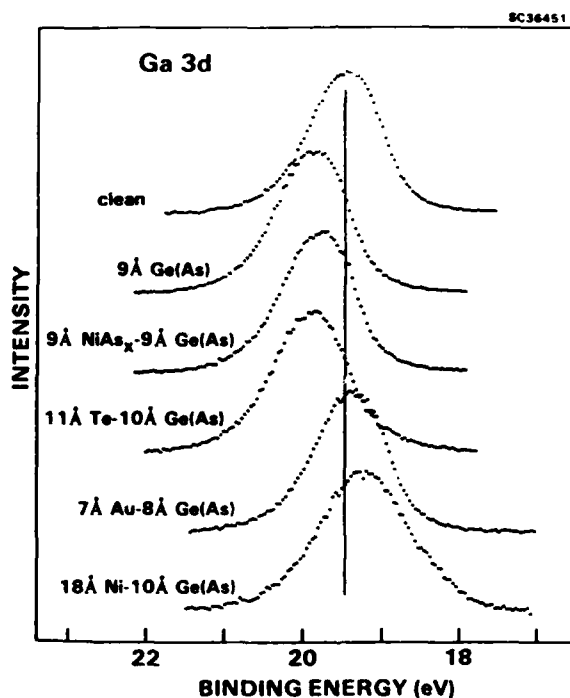22   20   18

BINDING ENERGY (eV)

Fig. 7   XPS Ga3d core level spectra for various thin overlayer structures on initially clean GaAs(100) surfaces. Upper three spectra are for successive depositions on the same sample.

After deposition of 9Å of Ge onto the clean GaAs surface at 250°C and in 1×10^7 Torr As_4 overpressure, the Ga3d peak shifts 0.43 eV to higher binding energy (compare upper two peaks). This shift represents an increase in E_F^1 to 1.10 eV. The E_F^1 for a thin Ge overlayer on clean GaAs will be defined as E_F^1(Ge) and the E_F^1(Ge) data are tabulated in Table 2. An E_F^1 of 1.10 eV corresponds to $\phi_B = 0.33$ eV which would be attractive for tunneling ohmic contact applications if it can be preserved upon deposition of additional contact material. The third and fourth spectra (from the top) in Fig. 7 demonstrate that the low band bending can still be preserved in certain cases. The third spectrum is for 9Å of $NiAs_x$ deposited onto the 9Å Ge(As) overlayer where E_F^1(Ge) = 1.1 eV. Essentially no change in the Ga3d energy, and hence no change in E_F^1, occurs. To test the generality of this result, another conductive nonmetal, Te, was used. When 11Å of Te is deposited onto a Ge(As) overlayer with high associated E_F^1 (Ge) (fourth spectrum), there is also no change in E_F^1. The situation is dramatically different when either Au or Ni is deposited directly onto a high E_F^1(Ge) overlayer of Ge(As) (lower two spectra in Fig. 7). In each case, E_F^1 shifted from E_F^1(Ge) = ~ 1.1 eV to E_F^1 = ~ 0.7 eV after the metal deposition; thus, the lower barrier condition was removed (the low binding energy shoulder in the last peak is due to a Ni-GaAs chemical reaction).

To investigate the correlation of XPS measured E_F^1 values with I-V measured ϕ_B, several kinds of model thick contact structures were formed. The types that include Ge are shown on the right side of Fig. 8; in each case, an initial Ge overlayer is followed (at room temperature) by the indicated depositions. Not shown are structures without the Ge layer (designated ideal), where Au, Ni, or $NiAs_x$ is deposited directly onto clean GaAs.

Figure 8 also shows representative I-V data (T = 295 or 150K, the lower measurement temperature was necessary for low ϕ_B) that demonstrate the wide range in ϕ_B which is associated with the different contact structures. The data were analyzed by the thermionic emission model (Section 2.2.1) and Table 2 lists the average ϕ_B and n values for the various interface structures (~ seven contacts per sample, < ±0.01 eV measurement uncertainty).

Table 2

Correlation of Interface Composition and Barrier Height for
Model Nonalloyed AuGeNi Contacts to GaAs

Interface Structure	Ge Depos. Temp. (°C)	$E_F^i(Ge)^a$ (eV)	$\phi_B^{b,c}$ (eV)	n
Au-NiAs$_x$-9Å Ge(As)	200	0.98	0.31^d	1.27
Au-NiAs$_x$-11Å Ge(As)	200	0.98	0.35^d	1.23
Au-NiAs$_x$-9Å Ge(As)	250	1.10	0.39^d	1.11
Au-100Å Te-10Å Ge(As)	200	1.07	0.23^e	1.33
Au-100Å Te-9Å Ge(As)	250	1.16	0.39^d	1.08
Au-100Å Te-7Å Ge(As)	325	1.05	0.36^d	1.10
Au-10Å Ge(As)	200	1.02	0.76	1.05
Au-8Å Ge(As)	250	0.98	0.61	1.05
Au-9Å Ge(As)	325	1.16	0.64	1.05
Ni-10Å Ge(As)	200	0.99	0.81	1.11
Au-100Å Te-9Å Ge	200	0.65	0.65	1.06
Au-9Å Ge	325	0.40	0.71	1.12
Au-100Å Te^f	---	--	0.79	1.02
NiAs$_x$-ideal	---	--	0.80	1.04
Ni-ideal	---	--	0.84	1.05
Au-ideal	---	--	0.89	1.05

a Ge overlayer only
b Includes image force correction, see Section 2.2.1
c Measured at T = 295K unless noted
d T = 150K
e T = 100K
f Reference 16

The Au-NiAs$_x$-Ge(As) and Au-Te-Ge(As) contacts that have a high E_F^i(Ge) (~ 1.0-1.2 eV) also have a low ϕ_B (~ 0.25-0.4 eV). In contrast, the Au-Ge(As) and Ni-Ge(As) contacts that have a similarly high E_F^i(Ge) value have, without an intervening NiAs$_x$ or Te layer, a high ϕ_B (~ 0.6-0.8 eV). These values for ϕ_B can be compared to those for the Au and Ni ideal contacts, ϕ_B(Au) = 0.89 eV and ϕ_B(Ni) = 0.84 eV. Thus, a high E_F^i state induced by a Ge(As) layer can be preserved by a NiAs$_x$ or Te layer that prevents Au or Ni from reaching the Ge-GaAs interface.

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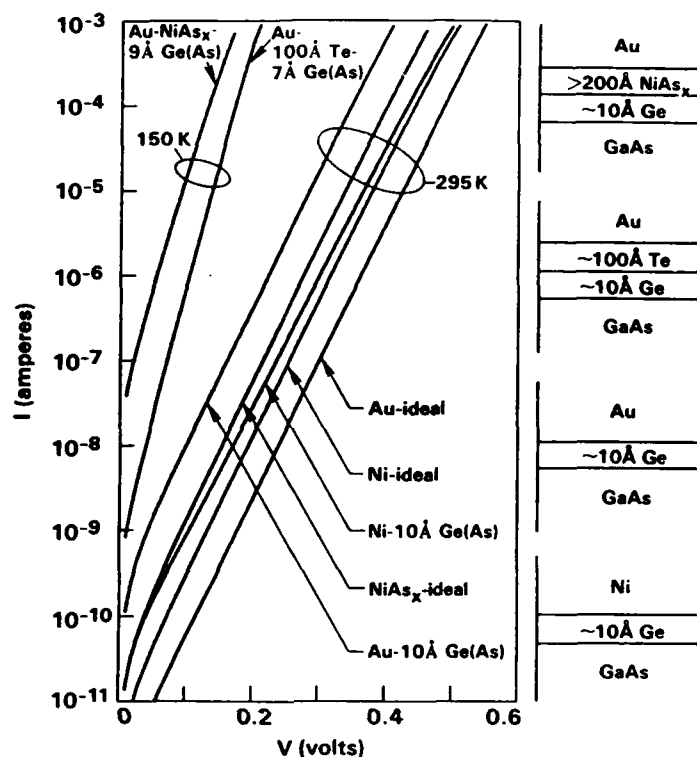
Fig. 8   Representative I-V data for a selection of contacts to GaAs that
have a variety of structures (contact area = 5.07×10^{-4} cm²).
Multilayered contact structures are shown schematically on right.

The $NiAs_x$-ideal and the Au-100Å Te contacts have ϕ_B = 0.79-0.80 eV, which
corresponds to E_F^i = 0.63-0.64 eV; this value of E_F^i is essentially that of the clean GaAs
surface.   Thus, $NiAs_x$ and Te have no effect on the Ge-GaAs interface electronic
structure while also providing a conducting electrical contact (other nonmetal conductors
with this property are likely).

In a careful electron microscopy investigation[33] of alloyed AuGeNi contacts,
ρ_c was found to depend on the relative contact areas of several Ni_2GeAs, NiAs, and
Au(Ga,As) phases.   It was concluded that a low ρ_c is achieved when the Ni_2GeAs phase
dominates because of heightened Ge indiffusion while a higher ρ_c occurs when Au areas

predominate. The present results suggest an alternate explanation: the Ni_2GeAs and NiAs phases may actually be separated from the GaAs by a very thin layer (not yet observed) of interface Ge and are thus associated with a low ϕ_B (~ 0.25-0.4 eV); the Au phase is associated with a high ϕ_B (~ 0.7-0.9 eV). Consequently, with this model, the minimum ρ_c for an alloyed AuGeNi ohmic contact is obtained when the interface area of phases associated with a low ϕ_B is greatest.

The large variation in ϕ_B, from ~ 0.25 to 0.9 eV, for the different model interface structures suggests that low ρ_c nonalloyed ohmic contacts that use Au, Ge, and Ni can be made to n^+-GaAs ($N_D > 5 \times 10^{18}$ cm^{-3}) if interface composition is controlled to minimize ϕ_B. For example, a properly fabricated $Au\text{-}NiAs_x\text{-}Ge(As)$ contact should have a low ϕ_B over the entire contact area. The ~ 0.65 eV range in ϕ_B also has implications for GaAs Schottky barrier models in that ϕ_B at GaAs interfaces cannot be assumed a priori to be restricted to values of ~ 0.7-0.9 eV.

4.1.3   TLM Measurements

As noted in Section 4.1.2, a properly fabricated $Au\text{-}NiAs_x\text{-}Ge(As)$ contact to n-GaAs should have a low ϕ_B over the entire contact area and would be expected to exhibit a low ρ_c. A contact that consisted of 10^3Å Au - ~ 500Å $NiAs_x$ - 10Å Ge(As) was fabricated on an MBE sample with a 1500Å n-type GaAs layer ($N_D = 2.3 \times 10^{18}$ cm^{-3}). The Ge(As) was deposited at 250°C. XPS measurements obtained following the 10Å Ge(As) deposition indicated that E_F^i was 1.0 eV which gives $\phi_B = 0.43$ eV.

An array of TLM test patterns was defined as described in Section 2.2.2. The data plotted in Fig. 9 are the average of data obtained from five patterns (there was only a very minor variation in the sample-to-sample data). R was measured at a current of 1 mA (sample ohmic behavior was confirmed by repeating a measurement at 0.1 mA with no change in measured R observed). The R vs L data have been least squares fit to a straight line to determine R_s and L_T. As discussed previously, $\rho_c = R_s L_T^2$. The uppermost plot in Fig. 9 is for the as-formed contacts. The three subsequent data sets are after 5 min rapid thermal anneals (in argon) at 300, 400 and 500°C, respectively. The values of ρ_c derived from these data are listed in Table 3. The sharp decrease in ρ_c after

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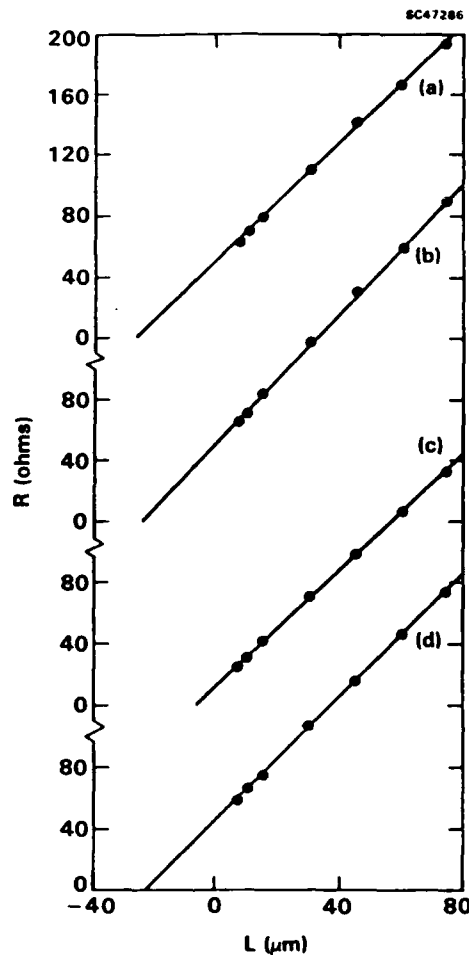
Fig. 9   TLM measurements for a 10^3Å Au-500Å NiAs$_x$-10Å Ge(As) ohmic contact
to n-GaAs (2.3×10^{18} cm^{-3}). Test pattern is shown schematically in
Fig. 4. (a) Initially fabricated sample, (b) annealed 300°C, 5 min,
(c) annealed 400°C, 5 min, and (d) annealed 500°C, 5 min.

the 400°C anneal may be attributed to Ge indiffusion causing an increase in n-type
doping near the contact interface. The increase in ρ_C after the 500°C anneal may be due
to Au indiffusion through the NiAs$_x$ that causes an increase in ϕ_B at the Ge-GaAs inter-
face, which would act to cancel the lowering of ρ_C by any Ge indiffusion; discoloration of
the Au metallization was noted after this anneal. A full understanding of this variation
in ρ_C with annealing, however, requires further study.

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Table 3

TLM Results for 10^3Å Au - - 500Å $NiAs_x$ - 10Å Ge(As)

Ohmic Contact to n-GaAs (100)

Anneal Temperature (°C)	R_s $(\Omega\square^{-1})$	L_T (µm)	ρ_c [b] $(\Omega\text{-cm}^2)$	Extrapolated [c] ρ_c $N_D = 1 \times 10^{19}\,\text{cm}^{-3}$ $(\Omega\text{-cm}^2)$	Extrapolated [c] ρ_c $N_D = 5 \times 10^{19}\,\text{cm}^{-3}$ $(\Omega\text{-cm}^2)$
Initial	240	13.3	4.3×10^{-4}	3×10^{-6}	2×10^{-7}
300 [a]	265	12.1	3.9×10^{-4}	---	---
400 [a]	237	3.11	2.3×10^{-5}	---	---
500 [a]	249	11.5	3.3×10^{-4}	---	---

a - annealed 5 min in argon
b - measured experimentally on $N_D = 2.3 \times 10^{18}\,\text{cm}^{-3}$ sample
c - extrapolation based on model of Ref. 34

Because practical nonalloyed ohmic contacts should be formed on heavier doped material than was used in the present case, extrapolated values of ρ_c at higher values of N_D are also given in Table 3. We obtained these predicted values by assuming a simplified model in which ρ_c is approximated in the form $\rho_c \sim \exp(C\phi_B N_D^{-1/2})$. A value for the constant C of 3.4×10^{-10} was derived from a curve ($\phi_B = 0.6$ eV) calculated in the tunneling model given in Ref. 34. This value of C and $\phi_B = 0.43$ eV were used to extrapolate the measured value of $\rho_c = 4.3 \times 10^{-4}\,\Omega\text{-cm}^2$ at $N_D = 2.3 \times 10^{18}\,\text{cm}^{-3}$.

4.2   Si Overlayers

As indicated in Section 4.1.1, the interface heterojunction band alignment characteristics appear to be responsible for the limits to the range of E_F^i values observed at the Ge/GaAs contacts. Because Si has a larger band gap than Ge, a wider range of E_F^i values might be obtained for UTHL contacts utilizing Si. Improved thermal stability might also be expected for Si contacts. Section 4.2.1 describes E_F^i measurements for Si UTHL contacts to n-GaAs and Section 4.2.2 reports I-V and C-V characterization of these contacts.

4.2.1 E_F^i Measurements

The range over which E_F^i in n-GaAs could be varied by using heavily doped n- or p-type Si overlayers was investigated. The Si overlayer thickness was in the 10-30Å range. Large E_F^i values were obtained by using heavily n-type doped Si layers (P or As dopants) while small E_F^i values were observed by using p-type doped Si layers (Ga or B dopants).

Si layers of ~ 10-30Å thickness were deposited at ~ 0.1Å/s onto clean GaAs surfaces held between 200 and 350°C (measurement of layer thickness was by noting the attenuation of the As3d peak from the underlying GaAs). For the B-doped Si layers, designated Si(B), material from the Si source was evaporated in vacuum. The procedure for the Ga-doped layers, Si(Ga), was somewhat more complex. The same Si source as for the Si(B) layers was used. Gallium was introduced into the Si by depositing a monolayer of Ga during the first few seconds of Si growth. This amount of Ga is more than can be incorporated into the Si in the thickness range used, which ensures that sufficient Ga is available to produce degeneracy. The most consistent low E_F^i Si(Ga)-GaAs interfaces were obtained when the chamber was back-filled with ~ 2×10^{-6} Torr H_2 during the Si deposition. Evidently, the hydrogen assists in the p-type doping process by minimizing the number of electrically active deep levels in the Si, but the precise mechanism(s) involved is not obvious. Silicon layers with incorporated P or As, Si(P) and Si(As), were obtained by evaporation of lightly n-type (P) Si in an ~ 2×10^{-6} Torr P_2 or 10^{-7} Torr As_4 background pressure.

Figure 10 shows representative As3d core level spectra to demonstrate the range in E_F^i that results from Si(P), Si(B), and Si(Ga) overlayers deposited onto clean GaAs (100) surfaces (peak heights are normalized). The upper two peaks are for the same sample. Thus, the vertical line that indicates the center (midpoint of the width at half-maximum) of the clean surface As3d peak at $E_{As3d} = 41.52$ eV corresponds to E_F^i (clean) = 0.78 eV. Deposition of a 14Å Si(P) overlayer onto this clean surface results in a 0.30 eV increase in binding energy to $E_{As3d} = 41.82$ eV, which is a E_F^i increase to $E_F^i = 1.08$ eV. In contrast, overlayers of Si(B) (third peak, $E_{As3d} = 41.24$ eV) and Si(Ga) (bottom peak, $E_{As3d} = 41.07$ eV) have a decrease in E_B relative to the clean surface, which is thus a E_F^i decrease to 0.50 and 0.33 eV, respectively.

Fig. 10   XPS As3d core level spectra for thin p-type and thin n-type Si layers deposited on clean n-type GaAs(100) surfaces.

The Ga3d core level peak was used to characterize the Si(As) overlayer on n-GaAs to avoid possible overlap of As3d lines from the GaAs substrate and the overlayer. These data are shown in Fig. 5(f) for a 14Å layer of Si deposited at 250°C.

Table 4 lists E_F^1 data for a number of samples in which Si(Ga), Si(B), Si(P), and Si(As) overlayers were deposited onto clean GaAs surfaces. The maximum range in E_F^1 for the Si-GaAs interfaces in Table 4 is 0.90 eV.

Low E_F^1 (high ϕ_B) values have been obained both with Ga and B heavily doped Si layers and high E_F^1 (low ϕ_B) values both with P and with As heavily doped layers (in principle, the Si layer should be degenerate and undepleted). Deposition temperatures between 200 and 350°C were used. A LEED pattern was observed for the 350°C growth which indicated epitaxy, but the lower temperature growths were either amorphous or polycrystalline. (LEED studies of Si growth on Si (100) have demonstrated epitaxy as low

Table 4

Interface Fermi Energy E_F^1 After Deposition of Various
Thin Si Layers Which Contain n-Type or p-Type Impurities
onto Clean n-Type GaAs(100) Surfaces

Impurity	Si Thickness[a] (Å)	E_{As3d}[b] (eV)	E_{Ga3d}[c] (eV)	E_F^1 (eV)
Ga	17	41.13	---	0.39
Ga	22	41.07	---	0.33
Ga	26	41.21	---	0.47
Ga	28	41.15	---	0.41
B	11[d]	41.24	---	0.50
B	24[d]	41.28	---	0.54
B	25[e]	41.23	---	0.49
P	14	41.82	---	1.08
P	25	41.84	---	1.10
As	14	---	19.98	1.23

a Except as noted, Si deposited at 250°C.
b As3d binding energy in GaAs with Si overlayer.
c Ga3d binding energy in GaAs with Si overlayer.
d 200°C.
e 350°C.

as 300°C[35]). Thus, neither a precise Si growth temperature (although the lower and upper limits have not been determined) nor a particular Si impurity are crucial. The large lattice mismatch of Si and GaAs and the generally nonepitaxial nature of the Si layers also show that the degree of Si-GaAs interface perfection is unimportant. The essential condition influencing E_F^1 at the Si-GaAs interface is that the Si be heavily either n-type or p-type.

Some difficulty was encountered in growing sufficiently heavily p-type Si films. The results with the B dopant were erratic with the method employed and there were some samples where the Si-GaAs E_F^1 was not low because the Si apparently failed to be heavily p-type. Although lower E_F^1 values were obtained with Ga, this should not be considered an inherent limitation of using B as a dopant but rather a requirement for good control over the Si dopant incorporation process. In this respect, the procedure for the Ga-doped films yielded better consistency in producing low E_F^1 interfaces, although

the importance of the hydrogen background needs to be clarified. On the other hand, heavily n-type Si by P or As incorporation was readily obtained. Under the conditions used, the Si(P) layer had a large P excess detected by XPS; the amount of P can probably be controlled by changing the level of P overpressure or the substrate temperature.

The E_F^1 data from Table 4 are plotted in Fig. 11. Also shown in this figure by dashed lines are the E_V and E_C positions of Si measured at Si/GaAs[36] heterojunction interfaces. Similar to the Ge overlayer results discussed in Section 4.1.1, the range in E_F^1 values observed for Si overlayers seems to be bounded by the Si band gap. A range of 0.76 eV in E_F^1 was observed for n- or p-type Ge layers on n-GaAs in Table 1. This range is similar to the 0.66 eV band gap of Ge and consistent with the Ge-GaAs heterojunction band lineup. A range of 0.9 eV in E_F^1 was observed for n- or p-type Si layers on n-GaAs in Table 4. This range is somewhat less than would be predicted by the 1.12 eV crystalline Si band gap. Thus, an additional increase in E_F^1 range at Si/GaAs interfaces of ~ 0.2 eV is probable by refinement of the Si deposition process.

It is usually assumed that the fairly narrow range of pinning positions observed at most GaAs interfaces is associated with acceptor and donor interface states closely spaced in energy.[12,37] The results of this work suggest that these states can be saturated with carriers from a heavily doped semiconductor overlayer so as to move E_F^1 from the GaAs pinning level to near the dopant level in the overlayer (i.e., near the overlayer band edges). Thus, the band alignment characteristics of the Ge/GaAs and Si/GaAs heterojunction interfaces are what determines E_F^1 at a UTHL contact.

In Section 4.1.2, metal deposition on UTHL contacts that involved Ge was shown to affect E_F^1 . Experiments were carried out to determine variations in E_F^1 after thin (~ 10-20Å) metal depositions on Si overlayers. The results of XPS measurements on As3d core levels are shown in Fig. 12 for Au and Ti depositions on Si(Ga) overlayers. The top three spectra are for sequential treatments to the same sample; the bottom peak is for the indicated two overlayers (the peak heights are normalized). The vertical line indicates the center (half width at half maximum) of the As3d peak. Deposition of 22Å of Si(Ga) onto the clean n-GaAs surface caused an 0.51 eV decrease of the As3d binding energy to 41.07 eV which corresponds to E_F^1 = 0.33 eV (compare the upper two peaks in Fig. 12). Similar E_F^1 data for other Si(Ga) and Si(P) overlayer samples are given in
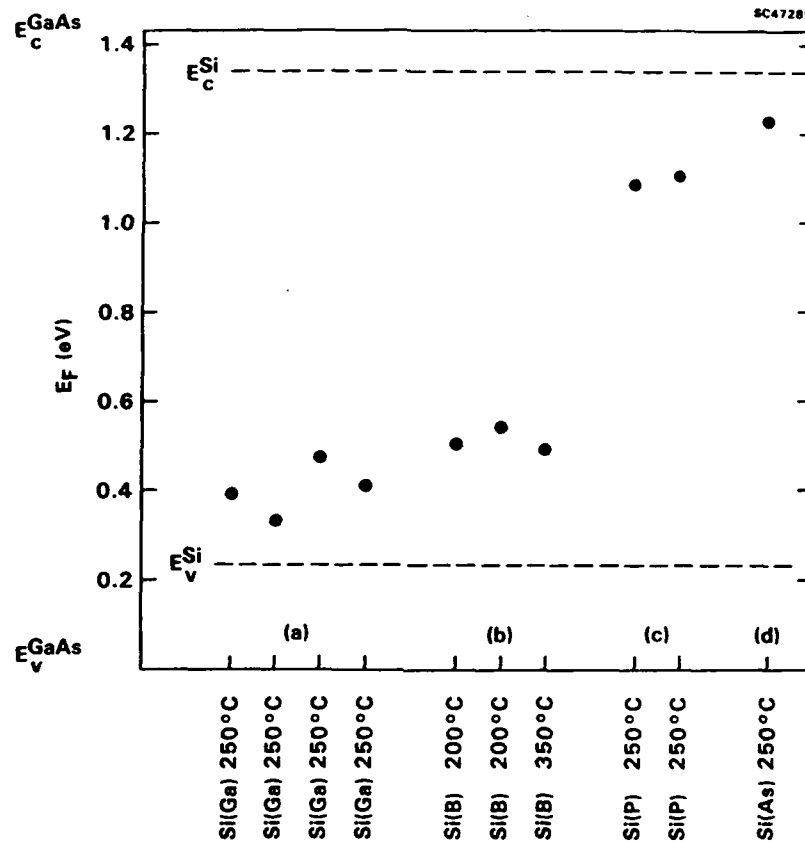
Fig. 11   Summary of several E_F^i measurements with Si overlayers. Overlayer thicknesses ranged from 11 to 28Å and are given in Table 4. Conditions used to incorporate dopants are specified in text. Silicon deposition temperatures are noted in figure. Dopants used were (a) Ga, (b) B, (c) P and (d) As.

Table 5.   As shown in the third spectrum of Fig. 12, deposition of an ~ 9Å thick Au overlayer essentially did not change E_F^i for the 22Å Si(Ga) sample; E_F^i in this case was 0.32 eV (see Table 5). Similarly, the bottom As3d peak at 41.12 eV (E_F^i = 0.38 eV) is for a 15Å Ti overlayer on the 17Å Si(Ga)-GaAs interface. Thus, deposition of Au or Ti does not increase the low E_F^i value established by the Si(Ga) layer. Deposition of Au onto Si(P) overlayer samples, however, caused an ~ 0.1 eV decrease in E_F^i. A large, ~ 1 eV, barrier
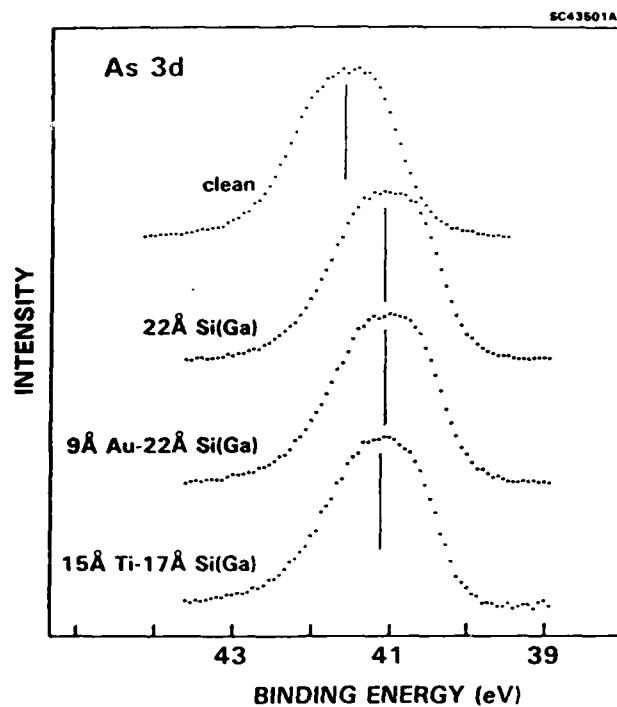
Fig. 12   XPS As3d core level spectra for various thin overlayers on clean n-type GaAs(100) surfaces.

Table 5

XPS Measured E_F^i After Deposition of Thin Si Overlayers

and After Subsequent Deposition of Thin Metal Overlayers

Contact	Silicon Overlayer E_F^i (eV)	Metal-Silicon Overlayer E_F^i (eV)
Au-22Å Si(Ga)	0.33	0.32
Ti-17Å Si(Ga)	0.39	0.38
Ti-26Å Si(Ga)	0.47	0.42
Au-14Å Si(P)	1.08	1.00
Au-25Å Si(P)	1.10	1.01

(ϕ_B = 1.43 eV - E_F^i) is therefore predicted for thick contacts to Si(Ga)-GaAs and a small ~ 0.4 eV barrier for contacts to Si(P)-GaAs.

The ~ 0.1 eV decrease in E_F^i observed for Au deposited on Si(P)-GaAs samples may occur for other metals. For ohmic contact applications to n-GaAs, it may be desirable to avoid this decrease. It is likely that the highest E_F^i at Si(n-type)-GaAs interfaces can be retained by interposition of a thin nonmetal electrical conductor between the contact metal and the Si (n-type)-GaAs interface. This was the approach used to maintain high E_F^i values at Ge(As)-GaAs UTHL contacts for example by using a NiAs$_x$ conducting diffusion barrier layer (see Section 4.1.2).

4.2.2   Electrical Characterization of Contacts

Thick (~ 10^3Å) metal layer contacts were also formed on ~ 20Å Si-GaAs samples to allow I-V and C-V measurements. Representative I-V data for thick metal Cr-28Å Si(Ga) and Ti-17Å Si(Ga) contacts are plotted in Fig. 13. Data for Au-22Å Si(Ga) contacts were also obtained but are not shown because of overlap with the Cr-Si(Ga) data. For comparison, I-V data for ideal contacts of these metals (metal deposited onto a clean n-GaAs surface) are also shown. These data were analyzed by using the thermionic emission model and results are given in Table 6. In several cases, XPS was used to measure the barrier height (ϕ_B^{XPS}) on thin metal-Si-GaAs samples prior to deposition (in situ) of the thick metal (~ 10^3Å) overlayers. The ϕ_B^{XPS} values are also given in Table 6. The significant increase in ϕ_B for the metal-Si(Ga) contacts compared to the respective ideal contacts is obvious from Fig. 13 and Table 1. In addition, the metal-Si(Ga) ϕ_B is independent of the contact metal, which is in contrast with the ideal contacts.

The variation in I-V characteristics that can be achieved by changing the doping characteristics of the thin Si layer is demonstrated in Fig. 14. Representative I-V data for thick metal Au-22Å Si(Ga), Cr-24Å Si(B), and Au-?5Å Si(P) contacts are shown. Again for comparison, data for ideal contacts are also presented. A significant increase in ϕ_B is apparent for Si(Ga) and Si(B) UTHL contacts as is a significant decrease for the Si(P) contact. Table 6 gives the average n and ϕ_B^{IV} measured for these contacts.
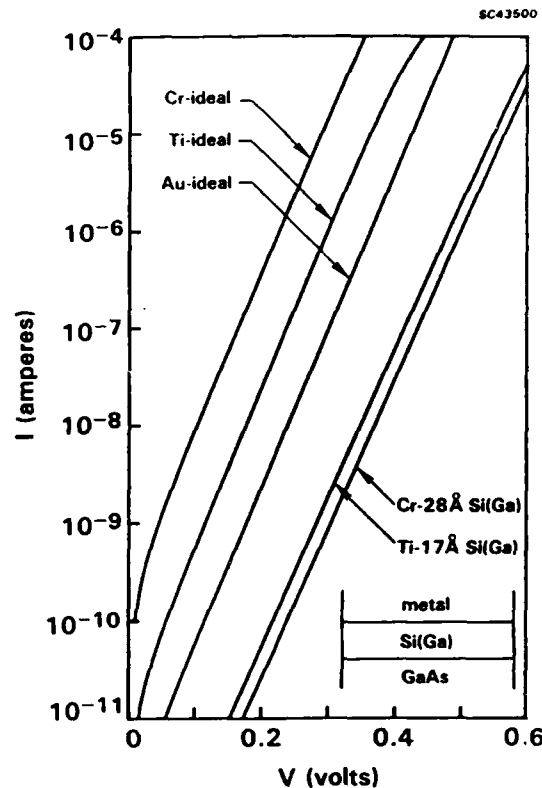
Fig. 13   Representative I-V data for Cr-Si(Ga) and Ti-Si(Ga) contacts compared to corresponding ideal contacts (Au-Si(Ga) data not shown because of overlap with Cr-Si(Ga) data). Contact area = 5.07×10^{-4} cm^2.

Representative C-V data for the Au-Si(Ga), Au-Si(P), and Au-ideal contacts are shown in the $1/C^2$ vs V plots of Fig. 15. The C-V data for the other contact samples were similar in form. The average ϕ_B^{CV} measured for each sample is listed in Table 6.

The I-V and C-V electrical measurements of ϕ_B on thick contacts are consistent with the $E_F^i(\phi_B)$ values measured by XPS with thin overlayers. Why ϕ_B^{CV} is ~ 0.1 eV $> \phi_B^{IV}$ for the Cr and Ti contacts with Si(Ga) and Si(B) interlayers and an opposite sign difference of 0.07 eV is measured for the Au-Si(P) contact is not clear. The agreement between I-V and C-V values for the Au-Si(Ga) contact, however, indicates that such disparities are not an intrinsic characteristic of all metal-Si-GaAs contacts. Since the

Table 6

Schottky Barrier Height ϕ_B of Metal Contacts to GaAs
that Include a Thin Si Interface Layer

Contact	XPS ϕ_B (eV)	n	IV ϕ_B a (eV)	CV ϕ_B (eV)
Au-22Å Si(Ga)	1.11	1.08	1.01	1.01
Cr-28Å Si(Ga)	----	1.11	0.99	1.10
Ti-17Å Si(Ga)	1.05	1.11	0.98	1.14
Ti-26Å Si(Ga)	1.01	1.10	0.97	1.06
Cr-24Å Si(B)	----	1.09	0.92	0.97
Au-14Å Si(P)	0.43	1.05	0.53	0.46
Au-25Å Si(P)	0.42	1.06	0.49	0.42
Au-ideal		1.05	0.89	
Cr-ideal		1.05	0.76	
Ti-ideal		1.04	0.83	

a   Includes image force correction.

discrepancies are comparatively minor and may be an artifact of the C-V model, for discussion purposes, the I-V values will be used: for the thick Si(Ga) contacts ϕ_B = 1.0 eV; for the Cr-Si(B) contact ϕ_B = 0.92 eV; and for the Au-Si(P) contact ϕ_B = 0.5 eV. The I-V ideality factors are acceptably small. Compared to the respective ideal contacts, the ϕ_B increase ranges from 0.1 eV (Au) to 0.23 eV (Cr) while the ϕ_B decrease for Au is 0.4 eV. By use of the metal-Si(p-type)-GaAs structure, ϕ_B can be made essentially independent of the contact metal.

The XPS measurements show that the wide range in ϕ_B for these metal-Si contacts is a direct consequence of the wide range in E_F^i that can be induced at the Si-GaAs interface. This mechanism for achieving a wide range in ϕ_B is thus quite unlike methods[38] in which a variable effective barrier height is created by tailoring the impurity profile, and therefore the potential, in the GaAs depletion region adjacent to the metal-GaAs interface where ϕ_B itself remains constant.
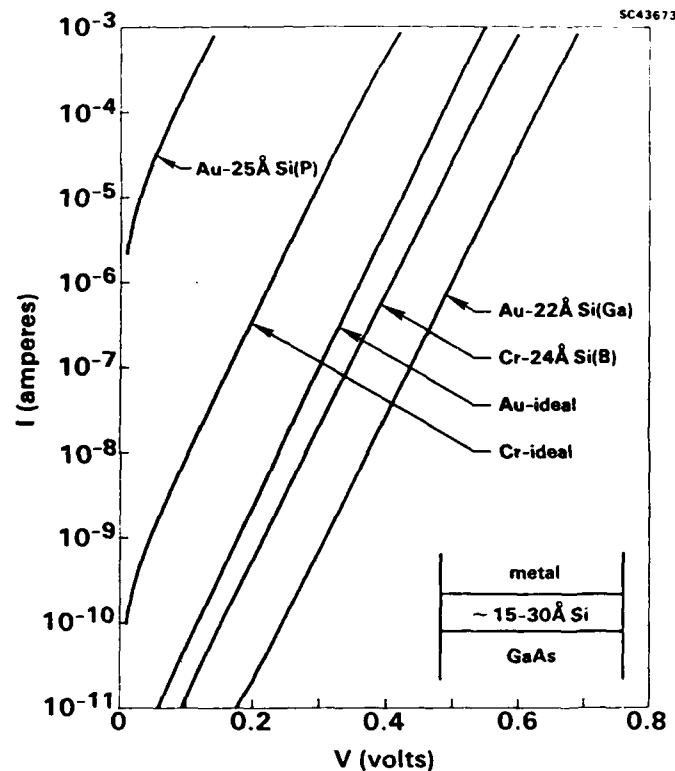
Fig. 14   Representative I-V data for Au-Si(Ga), Cr-Si(B), and Au-Si(P) contacts compared to Au-ideal and Cr-ideal contacts (contact area = 5.07×10^{-4} cm²).

Our results offer a possible basis for understanding the high barrier measured for thick amorphous Si-Ge-B contacts[39] to GaAs. If heavily p-type material in intimate contact with the GaAs was produced by the chemical vapor deposition process that was used, then E_F^1 may have been unpinned in the same way as at the Si(Ga)-GaAs interfaces described here.

The low barrier contacts obtained by using Si(n-type) interfaces should be useful in the design of ohmic contacts to n-GaAs. Because a high ϕ_B contact to n-GaAs should correspond to a low ϕ_B contact to p-GaAs, the high barrier contacts obtained by using Si(p-type) interlayers should be of use in the design of nonalloyed ohmic contacts to p-GaAs.
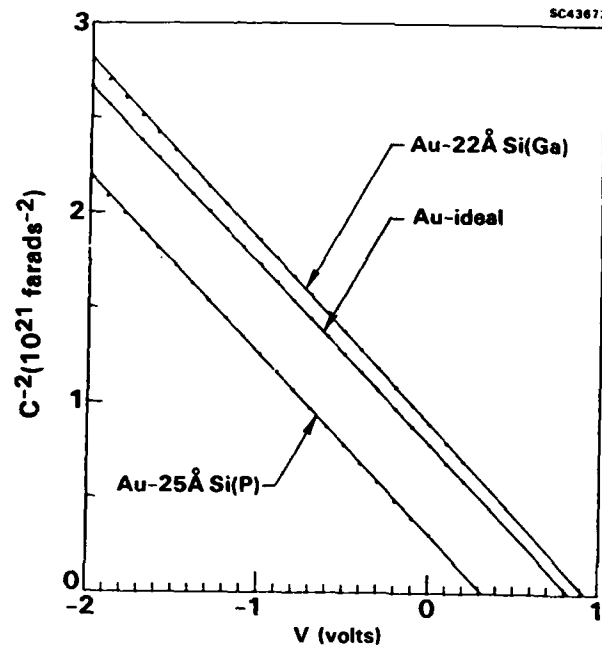
Fig. 15 Representative C-V data for Au-Si(Ga), Au-Si(P), and Au-ideal contacts. Line is least squares fit extrapolation to V_i.

Like GaAs, other III-V compound semiconductors (InP, for example) tend to have a limited range of ϕ_B for metal contacts. If the mechanism that restricts ϕ_B in other III-V semiconductors is analogous to that for GaAs, the present results suggest that appropriately doped Si or Ge interlayers will also increase the ϕ_B range for metal contacts to such semiconductors.

5.0 SUMMARY

A new approach for fabricating nonalloyed ohmic contacts to GaAs has been developed. The approach uses heavily doped ultrathin heterojunction layers (UTHL) of Ge or Si in contact with GaAs to alter the GaAs interface Fermi level position (E_F^i); typical Ge or Si layer thicknesses are 15-30Å.

The most common method of forming an ohmic contact to GaAs involves tunneling across a thin barrier region. For a tunneling ohmic contact, the specific contact resistance (ρ_c) depends exponentially on Schottky barrier height (ϕ_B). Thus, if the barrier height is reduced, a substantial reduction in ρ_c can be achieved. Most metal contacts to n-GaAs exhibit ϕ_B in the 0.7-0.9 eV range which corresponds to a 0.7-0.5 eV range in E_F^i. By using thin Ge or Si layers heavily doped n-type with As or P, E_F^i values between 1.0 and 1.2 could be obtained. For thin Si layers heavily doped p-type with Ga or B, or for vacuum-deposited Ge layers (normally heavily p-type), E_F^i values in GaAs ranged from 0.3 to 0.5 eV. Thus, it is possible to substantially extend the range of ϕ_B that can be obtained at a n-GaAs interface.

If the high E_F^i (low ϕ_B) n-GaAs interfaces can be retained in thick metallizations, they should be useful for ohmic contacts. Low barrier UTHL contacts to n-GaAs were demonstrated by both I-V and C-V measurements. To retain the high E_F^i values at Ge(Ga) - GaAs interfaces, it was necessary to interpose a thin nonmetal electrically conducting barrier (e.g., $NiAs_x$) between the contact metal and the Ge(As) layer to prevent the metal from reaching the GaAs interface. Although metallization of Si(P)-GaAs interfaces did not drastically reduce E_F^i, it is likely that the highest E_F^i at Si(n-type)-GaAs interfaces can also best be retained by using a nonmetallic electrically conducting barrier layer. With a nonalloyed Au-$NiAs_x$-GaAs UTHL contact structure, a $\rho_c = 4 \times 10^{-4}$ Ω-cm^2 was measured for a GaAs sample with donor concentration (N_D) = 2×10^{18} cm^{-3}; extrapolating this result to $N_D = 5 \times 10^{19}$ cm^{-3}, which is more typical of a practical n-GaAs ohmic contact, suggests that $\rho_c = 2 \times 10^{-7}$ Ω-cm^2 would be obtained for the UTHL contact. At 400°C and above, the Au-$NiAs_x$-GaAs UTHL contact was not stable which indicates the need to use thermodynamically stable components in future UTHL contact designs for high temperature applications.

High barrier UTHL contacts to n-GaAs were demonstrated by I-V and C-V measurements. For metallizations to Si(Ga)-GaAs UTHL contacts, an unusually large ϕ_B of ~ 1.0 eV was observed. Because a large ϕ_B to n-GaAs should correspond to a low ϕ_B to p-GaAs, the UTHL method of E_F^i modification should be applicable for p-GaAs ohmic contact design.

It is usually assumed that the fairly narrow range of pinning positions observed at most GaAs interfaces is associated with a large concentration of acceptor and donor states closely spaced in energy near midgap. The variation in GaAs E_F^i obtained by using heavily doped Ge or Si layers suggests that these states can be saturated with carriers from a heavily doped semiconductor overlayer so as to move E_F^i from the usual mid gap GaAs pinning level to near the dopant level in the overlayer (i.e., near the overlayer band edges). Thus, the band alignment characteristics of the Ge/GaAs and Si/GaAs hetero-junction interfaces determine E_F^i at a UTHL contact.

The generality of the UTHL method for modifying E_F^i was demonstrated by forming both low and high ϕ_B contacts to n-GaAs. While low ϕ_B interfaces have ohmic contact applications, high ϕ_B interfaces have FET gate applications. The UTHL contact has a ϕ_B that is virtually independent of contact metallization. The proposed heterojunction model for UTHL contact formation offers a means to design stable high temperature contacts by using materials expected to be thermodynamically stable at elevated temperatures. Like GaAs, other III-V semiconductors (e.g., InP) tend to have a limited range of ϕ_B for metal contacts. If the mechanism that limits this range is analogous to GaAs, the UTHL contact method may have more general applicability.

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7.0 APPENDIX

This appendix contains four publications, three conference abstracts and two patent disclosures that were based on work supported by this contract.

Publications

1. "Correlation of Interface Composition and Barrier Height for Model AuGeNi Contacts to GaAs," J.R. Waldrop and R.W. Grant, Appl. Phys. Lett 50, 250 (1987).

2. "Variation of n-GaAs(100) Interface Fermi Level by Ge and Si Overlayers," R.W. Grant and J.R. Waldrop, J. Vac. Sci. Technol. B5, 1015 (1987).

3. "Metal Contacts to GaAs with 1 eV Schottky Barrier Height," J.R. Waldrop and R.W. Grant, Appl. Phys. Lett. 52, 1794 (1988).

4. "Wide Range of Schottky Barrier Height for Metal Contacts to GaAs Controlled by Si Interface Layers," J.R. Waldrop and R.W. Grant, J. Vac. Sci. Technol. B6, 1432 (1988).

Conference Abstracts

1. "Variations of GaAs(100) Interface Fermi Level for Model AuGeNi Ohmic Contacts," R.W. Grant and J.R. Waldrop, Physics and Chemistry of Semiconductor Interfaces Conference, Salt Lake City, UT, Jan 27-29, 1987.

2. "Large Range of Interface Fermi Energy in n-GaAs(100) Induced by Thin Si Layers," J.R. Waldrop and R.W. Grant, Physics and Chemistry of Semiconductor Interfaces Conference, Asilomar, CA, Feb 1-4, 1988.

3. "Effect of Si and Ge Interface Layers on the Schottky Barrier Height of Metal Contacts to GaAs," J.R. Waldrop and R.W. Grant, Materials Research Society Conference, San Diego, CA, April 24-29, 1989.

Patent Disclosures

1. "Design of Nonalloyed Ohmic Contacts with Low Barrier Heights," J.R. Waldrop and R.W. Grant.
2. "Method for Obtaining Metal Contacts with Large Schottky Barrier," J.R. Waldrop and R.W. Grant.

Correlation of interface composition and barrier height for model AuGeNi contacts to GaAs

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Model contacts to GaAs that include nonalloyed layered structures of Au, Ge, and Ni in various combinations are used to establish a correlation between interface composition and large changes in barrier height ϕ_B. The interface Fermi level E'_F and chemistry during initial contact formation were investigated by x-ray photoemission spectroscopy; the corresponding ϕ_B for the thick contact was obtained by current-voltage (I-V) measurement. The circumstances under which a thin (~ 10 Å) Ge layer at the GaAs interface can produce $\phi_B = \sim 0.25$–0.4 eV (as measured by I-V) are described. For all model contacts examined a ϕ_B range from ~ 0.25 to 0.9 eV is observed. This result questions the usual assumption of a relatively fixed ϕ_B of ~ 0.8 eV for the alloyed AuGeNi contact and offers an alternative explanation for the mechanism of ohmic contact formation. The conditions that define the exceptionally low ϕ_B contacts provide a guide for the design of nonalloyed tunnel ohmic contacts.

The alloyed AuGeNi metallization[1] is widely used as an ohmic contact to n-type GaAs. The complex contact structure consists of several phases whose individual size and composition depend on the alloying time and temperature.[2-5] The familiar ohmic contact tunneling[6] model that gives[7] $\rho_c \propto \exp(a\phi_B/N_D^{1/2})$, where ρ_c is the specific contact resistance, ϕ_B is the interface barrier height, N_D is the donor concentration in the GaAs ($> \sim 5 \times 10^{18}$ cm^{-3}), and $a = 5 \times 10^{10}$ cm$^{-3/2}$ eV^{-1}, is troublesome to apply quantitatively to the alloyed contact. This difficulty arises from not knowing precisely either ϕ_B or the effect of Ge, Au, or Ni indiffusion on N_D. It is usually assumed that ϕ_B is inevitably ~ 0.7–0.9 eV because the Schottky barrier height[8,9] for most metal contacts to GaAs is in this range. According to this viewpoint ρ_c is reduced by maximizing N_D. However, for certain thin (~ 10–40 Å) Ge overlayers on clean GaAs surfaces the interface Fermi energy E'_F can be > 1 eV.[10,11] Hence, if such a high E'_F state (low ϕ_B) can be attained in a tunnel AuGeNi ohmic contact then ρ_c would be substantially reduced for a given N_D.

This letter reports an investigation of model AuGeNi contacts to GaAs that involve layered structures designed to correlate interface composition with ϕ_B. The contacts were not alloyed to retain interfaces of controlled composition. The interface chemistry and E'_F during initial contact formation were observed by x-ray photoemission spectroscopy (XPS); the corresponding ϕ_B for a thick contact was obtained by current-voltage (I-V) measurement. Since the current transport for a tunnel contact depends on both ϕ_B and N_D, GaAs with N_D appropriate for thermionic emission transport ($< 10^{17}$ cm^{-3}) was used to simplify the I-V analysis.

The contact interfaces were prepared under ultrahigh vacuum conditions (10^{-10} Torr range base pressure) in an XPS system comprised of a HP5950A electron spectrometer ($h\nu = 1486.6$ eV monochromatic x-ray source, ~ 16 Å effective photoelectron escape depth) and attached custom sample preparation chamber. During initial contact formation XPS spectra of the Ga $3d$ and As $3d$ core level peaks in

the GaAs and of other core level peak spectra appropriate for a given interface composition were obtained. I-V data were obtained in 0.01 V forward bias increments.

The GaAs (100) material is liquid encapsulated Czochralski grown n type ($\sim 5 \times 10^{16}$ cm^{-3} Se). To prepare a sample, the GaAs is etched in fresh 4:1:1 H_2SO_4:H_2O_2:H_2O solution for ~ 30 s to remove polishing damage, mounted on a Mo plate with In and immediately put into the XPS system. The ~ 10 Å native oxide layer is removed by momentary heating, either in vacuum or in an As overpressure, to the minimum necessary temperature (~ 550 °C, which also forms an ohmic contact between the GaAs and the Mo plate). This thermally cleaned surface is ordered [displays a characteristic low-energy electron diffraction (LEED) pattern] and is shown by XPS to be free of oxygen, carbon, or other contaminants. The Ge, Au, and Ni were evaporated from W baskets; the As and Te sources were small quartz ovens. The NiAs layers were formed by depositing the Ni onto a room-temperature substrate in a 10^{-7}–10^{-6} Torr As overpressure [although XPS analysis indicates the resulting Ni and As layer is As rich, and thus a compound(s) of the form NiAs$_x$, for simplicity it will be referred to as NiAs]. After XPS analysis of thin overlayers, a total overlayer thickness of > 2000 Å was deposited. Circular 2.54×10^{-2} cm diameter contacts were defined by using photolithography and chemical etching.

The representative Ga $3d$ core level peak data plotted in Fig. 1 show how XPS was used to measure E'_F and to monitor composition during interface formation. The upper three spectra are after sequential treatments to the same sample; the lower three are for three other samples with the indicated overlayer structure (peak heights are normalized). The upper inset in Fig. 2 shows the relationship between the interface Ga $3d$ core level binding energy in GaAs and E'_F: $E'_F = E_{Ga\,3d} - 18.80$ eV, where $(E_{Ga\,3d} - E_v) = 18.80 \pm 0.03$ eV is the energy difference[12] between the Ga $3d$ core level and the valence-band maximum. Note that the binding energy E_B scale is referenced to the sample Fermi energy E_F (other details on the use of XPS to measure E'_F can be found
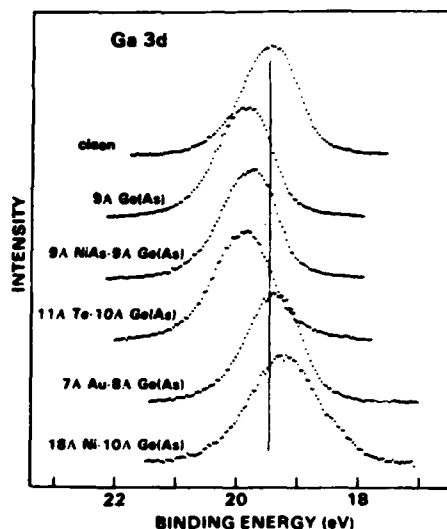
FIG. 1. XPS Ga 3d core level spectra for various thin overlayer structures on initially clean GaAs (100) surfaces. Upper three spectra are for successive depositions on the same sample.

elsewhere).[13] Thus, the vertical line in Fig. 1 that marks the center of the clean surface Ga 3d peak at 19.47 eV is for E'_F (clean) = 0.67 eV (the average for 16 samples is 0.66 eV, as indicated in Fig. 2).

After deposition of 9 Å of Ge onto the clean GaAs surface at 250 °C and in 1×10^{-7} Torr As overpressure the Ga 3d peak shifts 0.43 eV to higher binding energy (compare upper two peaks). This shift represents an *increase* in E'_F to 1.10 eV. The E'_F for a thin Ge overlayer on clean GaAs will be defined as E'_F (Ge). Figure 2 gives the value of E'_F (Ge) for 13 different samples in which ~10 Å of Ge was deposited onto clean GaAs (see lower inset) at several different substrate temperatures and As overpressure conditions. These E'_F (Ge) data are also tabulated in Table I.

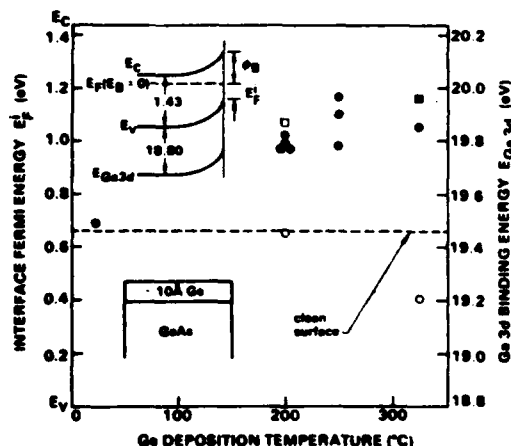For Ge deposited in a 200–325 °C temperature range under conditions where As incorporation occurs [designat-

ed Ge(As)], which presumably makes the Ge *n* type, E'_F (Ge) = 1.0–1.2 eV. A LEED pattern from the Ge was observed for these layers (with a high background at 200 °C). Room-temperature Ge deposition (no LEED pattern), or 200–325 °C Ge deposition on a vacuum cleaned surface without an As overpressure, yields E'_F (Ge) = 0.4 –0.7 eV.

The relation $\phi_B = 1.43$ eV $- E'_F$ indicates that barriers in the 0.2–0.4 eV range can be achieved if the low band bending state (high E'_F) can be preserved upon deposition of additional contact material. For example, the third (from top) spectrum in Fig. 1 is for 9 Å of NiAs deposited onto the 9 Å Ge(As) overlayer where E'_F (Ge) = 1.1 eV. Essentially no change in the Ga 3d energy, and hence no change in E'_F, occurs. To test the generality of this result another conductive nonmetal, Te, was used. When 11 Å of Te is deposited onto a Ge(As) overlayer with high associated E'_F (Ge) (fourth spectrum) there is also no change in E'_F. The situation is dramatically different when either Au or Ni is deposited directly onto a high E'_F (Ge) Ge(As) overlayer (lower two spectra in Fig. 1). In each case E'_F shifted from E'_F (Ge) = ~1.1 eV to E'_F = ~0.7 eV after the metal deposition; thus, the low barrier condition was removed (the low binding energy shoulder in the last peak is due to a Ni-GaAs chemical reaction).

Do the XPS measurements of E'_F shifts correlate with the I-V ϕ_B data for the same interfaces? To investigate this question several kinds of model thick contact structures were formed. The types that include Ge are shown on the right side of Fig. 3; in each case an initial Ge overlayer is followed (at room temperature) by the indicated deposi-

TABLE I. Correlation of interface composition and barrier height for model nonalloyed AuGeNi contacts to GaAs.

Interface structure	Ge depos. temp. (°C)	E'_F (Ge)[a] (eV)	ϕ_B[b] (eV)	n
Au-NiAs-9 Å Ge(As)	200	0.98	0.31[d]	1.27
Au-NiAs-11 Å Ge(As)	200	0.98	0.35[d]	1.23
Au-NiAs-9 Å Ge(As)	250	1.10	0.39[d]	1.11
Au-100 Å Te-10 Å Ge (As)	200	1.07	0.23[c]	1.33
Au-100 Å Te-9 Å Ge(As)	250	1.16	0.39[d]	1.08
Au-100 Å Te-7 Å Ge(As)	325	1.05	0.36[d]	1.10
Au-10 Å Ge(As)	200	1.02	0.76	1.05
Au-8 Å Ge(As)	250	0.98	0.61	1.05
Au-9 Å Ge(As)	325	1.16	0.64	1.05
Ni-10 Å Ge(As)	200	0.99	0.81	1.11
Au-100 Å Te-9 Å Ge	200	0.65	0.65	1.06
Au-9 Å Ge	325	0.40	0.71	1.12
Au-100 Å Te[f]	...	...	0.79	1.02
NiAs-ideal	...	...	0.80	1.04
Ni-ideal	...	...	0.84	1.05
Au-ideal	...	...	0.89	1.05

[a] Ge overlayer only.
[b] Includes image force correction, see text.
[c] Measured at T = 295 K unless noted.
[d] T = 150 K.
[e] T = 100 K.
[f] Reference 17.

FIG. 2. Interface Fermi energy E'_F (Ge) for thin (~10 Å) Ge overlayers deposited on GaAs (100) surfaces at several different temperatures. The closed circles and square are for 10^{-7} and 10^{-8} Torr As overpressure during Ge evaporation, respectively; the open circles are for a GaAs surface cleaned and Ge deposited in vacuum; the open square is for GaAs cleaned in 10^{-8} Torr As and Ge deposited in vacuum.

tions. Not shown are structures without the Ge layer (designated ideal) where Au, Ni, or NiAs is deposited directly onto clean GaAs.

Figure 3 also shows representative I-V data ($T = 295$ or 150 K, the lower measurement temperature was necessary for low ϕ_B) that demonstrate the wide range in ϕ_B which is associated with the different contact structures. The I-V data were analyzed by use of the thermionic emission model[14] for a Schottky barrier: $I = I_s \exp(qV/nkT)[1 - \exp(-qV/kT)]A$, where both the ideality factor n ($n \sim 1.02$ at $T = 295$ K is ideal; there is often, however, an increase in n at low T)[14] and I_s were determined by a least-squares fit. The barrier height ϕ_B is extracted from I_s by $I_s = SA^*T^2 \times \exp[-q(\phi_B - \Delta\phi)/kT]A$, where S is the contact area, $A^* = 8.16$ is the effective Richardson constant, and $\Delta\phi$ is the calculated[14] image force correction ($\Delta\phi = +0.04$ eV for $\phi_B \geqslant 0.7$ eV and $+0.03$ eV for $\phi_B < 0.7$ eV). Table I lists the average ϕ_B and n values for the various interface structures ($\sim$ seven contacts per sample, $< \pm 0.01$ eV measurement uncertainty).

The Au-NiAs-Ge(As) and Au-Te-Ge(As) contacts that have a high E_F'(Ge) (~ 1.0–1.2 eV) also have a low ϕ_B (~ 0.25–0.4 eV). In contrast, the Au-Ge(As) and Ni-Ge(As) contacts that have a similarly high E_F'(Ge) value have, without an intervening NiAs or Te layer, a high ϕ_B (~ 0.6–0.8 eV).[15] These values for ϕ_B can be compared to those for the Au and Ni[16] ideal contacts, ϕ_B(Au) = 0.89 and ϕ_B(Ni) = 0.84 eV, and the two contacts where E_F'(Ge) was 0.4 and 0.65 eV. Thus, a high E_F' state induced by a Ge(As) layer can be preserved by a NiAs or Te layer that prevents Au or Ni from reaching the Ge-GaAs interface.

The NiAs-ideal and the Au-100 Å Te[17] contacts have ϕ_B = 0.79–0.80 eV, which corresponds to $E_F' = 0.63$–0.64 eV; this value of E_F' is essentially that of the clean GaAs surface. Thus, NiAs and Te have no effect on the Ge-GaAs interface electronic structure while also providing a conducting elec-

trical contact (other nonmetal conductors with this property are likely).

In a careful electron microscopy investigation[4] of alloyed AuGeNi contacts ρ_c was found to depend on the relative contact areas of several Ni_2GeAs, NiAs, and Au(Ga,As) phases. It was concluded that a low ρ_c is achieved when the Ni_2GeAs phase dominates because of heightened Ge indiffusion while a higher ρ_c occurs when Au areas predominate. The present results suggest an alternate explanation: the Ni_2GeAs and NiAs phases may actually be separated from the GaAs by a very thin layer (not yet observed) of interface Ge and are thus associated with a low ϕ_B (~ 0.25–0.4 eV); the Au phase is associated with a high ϕ_B (~ 0.7–0.9 eV). Consequently, with this model the minimum ρ_c for an alloyed AuGeNi ohmic contact is obtained when the interface area of phases associated with a low ϕ_B is greatest.

The large variation in ϕ_B, from ~ 0.25 to 0.9 eV, for the different model interface structures suggests that low ρ_c nonalloyed ohmic contacts that use Au, Ge, and Ni can be made to n^+-GaAs ($N_D > 5 \times 10^{18}$ cm^{-1}) if interface composition is controlled to minimize ϕ_B. For example, a properly fabricated Au-NiAs-Ge(As) contact should have a low ϕ_B over the entire contact area.[18] The ~ 0.65 eV range in ϕ_B also has implications for GaAs Schottky barrier models in that ϕ_B at GaAs interfaces cannot be assumed a priori to be restricted to values of ~ 0.7–0.9 eV.

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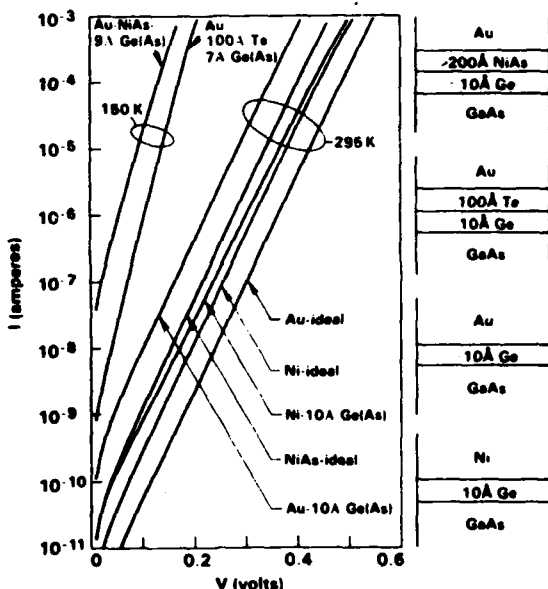
FIG. 3. Representative I-V data for a selection of contacts to GaAs that have a variety of structures (contact area = 5.07×10^{-4} cm^2). Multilayered contact structures are shown schematically on right.

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Variation of n-GaAs (100) interface Fermi level by Ge and Si overlayers

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The interface Fermi level (E_F^i) for interfaces that were formed by depositing thin (~ 10 Å) layers of Ge and Si onto heated GaAs (100) substrates was studied by x-ray photoelectron spectroscopy. The value of E_F^i for Ge overlayers (relative to the GaAs valence band maximum) could be varied from ~ 0.5 eV to ~ 1.2 eV by depositing the Ge in vacuum or by depositing it in an As_4 or P_2 background pressure ($\sim 10^{-7}$ Torr). These E_F^i values roughly correspond to the band edges of Ge at the Ge/GaAs heterojunction interface, which suggests that the dopant type in the Ge overlayer and band alignment play a significant role in determining E_F^i. A thin Si overlayer with incorporated As also exhibited an E_F^i of ~ 1.2 eV. The results suggest that heterojunction band alignment characteristics for Ge/GaAs and Si/GaAs based electrical contacts are important in determining the range over which E_F^i can be varied. The large E_F^i variation could have an application in the design of nonalloyed GaAs ohmic contacts.

I. INTRODUCTION

Metal contacts to n-GaAs generally have Schottky barrier heights (ϕ_B) of 0.7–0.9 eV[1-3]; the corresponding interface Fermi level position (E_F^i) is ~ 0.7–0.5 eV above the valence band maximum (E_v). In addition, oxidized n-GaAs surfaces[4] and thin Ge overlayers[5] can exhibit E_F^i values in this same range. Although most n-GaAs E_F^i positions are confined to the fairly narrow limits indicated above, growing evidence shows that at some n-GaAs interfaces much larger E_F^i values can be obtained.[6-11] An understanding of the factors that influence E_F^i would clarify the Fermi level (E_F) pinning mechanism and be significant for improved GaAs ohmic contact development, where large E_F^i values are desirable.

The most widely used ohmic contact to n-GaAs is the alloyed AuGeNi metallization.[12] Numerous studies have revealed that the heterogeneous contact structure consists of several phases, with phase size and composition dependent on alloying conditions.[13,14] The ohmic contact formation mechanism is not well-known. It is usually assumed that E_F^i at the GaAs interface is ~ 0.6 eV and that a tunneling contact is formed by heavy Ge donor doping of the GaAs near-interface region.[15] The tunneling contact model[16] has $\rho_c \sim \exp(C\phi_B N_D^{-1/2})$, where ρ_c is the specific contact resistance, N_D is the net donor concentration, and C is a constant. Thus, for a fixed ϕ_B (or E_F^i), ρ_c is minimized by maximizing N_D.

For certain thin (~ 10–40 Å) Ge overlayers on clean GaAs surfaces, E_F^i can be > 1 eV.[8,9] It has recently been demonstrated[17] by I–V measurements that this high E_F^i value can be retained for thick contacts formed under suitable conditions; a high E_F^i should make it possible to significantly reduce ρ_c for a given N_D. This paper reports further studies of E_F^i on n-GaAs (100), with the goal of investigating factors that can produce large E_F^i values.

II. EXPERIMENT

The interfaces studied were prepared in an ultrahigh vacuum (UHV) (base pressure 10^{-10} Torr) custom sample preparation chamber attached to a Hewlett–Packard (HP) 5950A x-ray photoelectron spectroscopy (XPS) system; a monochromatic AlKα ($h\nu = 1486.6$ eV) x-ray source was used and the effective photoelectron escape depth was ~ 16 Å. The bulk GaAs (100) material used was n-type (~ 3–5×10^{16} cm^{-3}). To prepare a sample, the GaAs was etched in $4H_2SO_4{:}H_2O_2{:}H_2O$ for ~ 30 s to remove polishing damage, mounted on a Mo plate with In and immediately inserted into the XPS system. The ~ 10 Å native oxide layer was removed by momentarily heating in vacuum to the minimum necessary temperature (~ 550 °C). This thermally cleaned surface is ordered [displays a characteristic low-energy electron diffraction (LEED) pattern] and shown by XPS to be free of oxygen, carbon, or other contaminants. To prepare an interface, thin layers of Ge or Si were deposited onto the thermally cleaned GaAs (100) substrates. The substrate temperatures were controlled between room temperature and 325 °C, and the depositions were performed in UHV or in background pressures of As_4 or P_2. The Ge and Si were evaporated from W baskets, while the As_4 source was a small quartz oven and the P_2 source was an InP crystal heated by a W wire coiled around it. Deposition rates for Ge and Si were ~ 0.1 Å/s. The deposited overlayer thickness was estimated from the GaAs substrate Ga3d core-level intensity attenuation.

During interface formation, XPS spectra of the Ga3d, As3d, and either the Ge3d or Si2p core-level peaks were obtained. The XPS measurement of E_F^i for all the interfaces is illustrated schematically in Fig. 1, where E_c^{GaAs} and E_v^{GaAs} are the GaAs conduction band minimum and valence band maximum, respectively, E_{Ga3d}^{GaAs} is the Ga3d core-level binding energy in GaAs [the binding energy (E_B) scale is 0 at E_F], and W is the depletion width. In all cases, the overlayer thicknesses studied were comparable to the Ga3d photoelectron escape depth and E_{Ga3d}^{GaAs} was used to measure E_F^i. For mid-10^{16} cm^{-3} n-type GaAs material, W is ~ 1000 Å, and thus GaAs band-bending does not complicate the measurement. To determine E_F^i, the relationship $E_F^i = E_{Ga3d}^{GaAs} - 18.75$ eV was used, where 18.75 ± 0.03 eV[19] is the E_B difference between E_{Ga3d}^{GaAs} and E_v^{GaAs}. At the conclusion of an

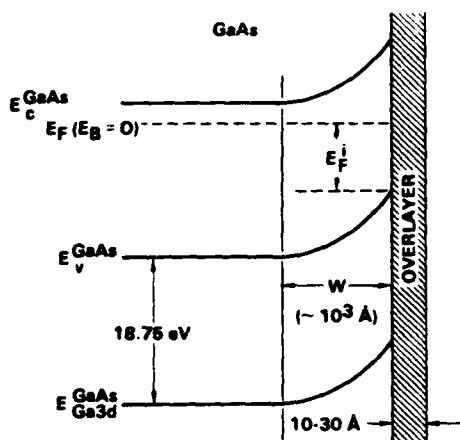FIG. 1. Schematic energy band diagram that illustrates the XPS measurement of E'_F for GaAs.
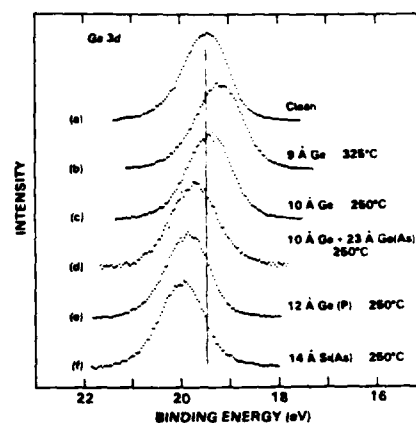

FIG. 2. XPS Ga3d core-level spectra for several GaAs (100) samples with thin overlayers. The overlayer composition and deposition temperatures are noted in the figure. The spectra shown as (c) and (d) are for the same sample, except for the additional Ge(As) layer.

interface characterization, a thick Au metal layer was evaporated from a W basket onto the sample surface and an absolute E'_F value was obtained by indexing the Au$4f_{7/2}$ XPS peak position to 84.00 eV.[18] Further details on the use of XPS to measure E'_F can be found elsewhere.[6]

III. RESULTS

Representative XPS Ga3d core-level spectra for several samples are compared in Fig. 2. A spectrum from a thermally cleaned surface is shown for reference in Fig. 2(a) (the vertical line shown in the figure marks the center of this Ga3d line). The two spectra shown in Figs. 2(b) and 2(c) are for GaAs samples on which thin layers of Ge were deposited in vacuum at 325 and 250 °C, respectively. A low energy electron diffraction (LEED) pattern was observed for the Ge layers deposited (either in vacuum or in the presence of an As₄ background pressure) in the 200–325 °C temperature range, although the pattern had a high background at 200 °C.[17] The Ga3d binding energy decrease noted in Figs. 2(b) and 2(c) spectra relative to the thermally clean surface represents a decrease in E'_F, and thus a corresponding increased band bending. The spectrum shown in Fig. 2(d) is for the same sample that was studied in Fig. 2(c), but with the addition of a 23-Å thick layer of Ge deposited at 250 °C under conditions (1×10^{-7} Torr As₄ background pressure) where As incorporation occurs [this layer is designated Ge(As)]. A marked shift to higher E_B (lower band bending) occurs.

Two additional spectra are shown in Figs. 2(e) and 2(f). The first is from a sample on which a 12-Å Ge layer was deposited at 250 °C in the presence of a 10^{-6}-Torr P₂ background. Figure 2(f) spectrum is from a sample on which a 14-Å layer of Si was deposited at 250 °C in the presence of a 10^{-7} Torr As₄ background pressure. Both samples have substantially lower band-bending than the thermally cleaned surface. The Si(As) overlayer did not exhibit a LEED pattern. Subsequent annealing of this sample to 400 °C for 1 min yielded a weak pattern. LEED studies of Si growth on Si (100) have demonstrated epitaxy as low as 300 °C.[20] Pre-

sumably, 250 °C is slightly too low to achieve epitaxy. Values of E_{Ga3d}^{GaAs} and of the corresponding E'_F are given in Table I for the samples noted in Fig. 2, and for several other samples included in this work (some of these results are from Ref. 17 and are included here for completeness).

IV. DISCUSSION

Several of the results listed in Table I are shown pictorially in Fig. 3. The overlayer characteristics are noted at the bottom of the figure, and the corresponding E'_F value is shown on the vertical scale. The positions of E_v^{GaAs} and E_c^{GaAs} are listed on the vertical scale ($E'_F = 0$ at E_v^{GaAs}). As will be noted below, the interface heterojunction band alignment characteristics appear to play a role in determining the observed E'_F positions. Thus, also shown in this figure by dashed lines are the E_v and E_c positions for Ge and Si measured at Ge/GaAs[21] and Si/GaAs[22] heterojunction interfaces.

The data shown in Fig. 3 are grouped into five sets (a)–(e). The first set (a) shows E'_F values obtained with Ge overlayers that were deposited in vacuum between 200 and 325 °C. The data indicate that band bending in the GaAs increases slightly with increasing Ge deposition temperature. Vacuum-deposited Ge is almost always found to be p-type,[23] independent of the substrate. The results shown in Fig. 3(a) suggest that the acceptor density (associated with either the deposition process and/or Ga incorporation from the substrate) increases with increasing deposition temperature. The Ge is degenerate p-type when vacuum deposited at 325 °C on thermally cleaned GaAs substrates, in agreement with previous results.[24] Exposure of the Ge overlayer grown at 325 °C to 30 L of As₄ with the sample held at 325 °C caused only a small (~0.06 eV) decrease in GaAs band bending, as indicated by the arrow in Fig. 3(a).

The E'_F values shown in Fig. 3(b) are for Ge(As) overlayers deposited between 200 and 325 °C. The net donor den-

TABLE I. Values of E^{GaAs}_{Ga3d} and E'_F for several n-GaAs(100) interfaces.

Sample No.	Overlayer	Deposition Temp. (°C)	Overlayer thickness (Å)	Background pressure during deposition (Torr)	E^{GaAs}_{Ga3d} (eV)	E'_F (eV)
1	Thermally clean (ave. of 16 samples)	...	...	...	19.46	0.71
2	Ge	200	9	Vacuum	19.45	0.70
3	Ge[a]	200	10	Vacuum	19.87	1.12
4	Ge	250	10	Vacuum	19.40	0.65
5	Sample No. 4 + Ge(As)	250	23	10^{-7} As$_4$	19.73	0.98
6	Ge	250	6	Vacuum	19.47	0.72
7	Sample No. 6 + Ge(As)	250	6	10^{-7} As$_4$	19.88	1.13
8	Ge	325	9	Vacuum	19.20	0.45
9	Sample No. 8 + Exposure to 30 L As$_4$ at 325 °C	...	...	...	19.26	0.51
10	Ge(As)	RT	26	10^{-7} As$_4$	19.49	0.74
11	Ge(As)	200	10	10^{-7} As$_4$	19.82	1.07
12	Ge(As)	200	7	10^{-7} As$_4$	19.79	1.04
13	Ge(As)[b]	200	9	10^{-7} As$_4$	19.78	1.03
14	Ge(As)	200	11	10^{-7} As$_4$	19.78	1.03
15	Ge(As)[a]	200	4	10^{-7} As$_4$	19.78	1.03
16	Ge(As)	250	9	10^{-7} As$_4$	19.96	1.21
17	Ge(As)	250	9	10^{-7} As$_4$	19.90	1.15
18	Ge(As)	250	8	10^{-7} As$_4$	19.78	1.03
19	Ge(As)	250	7	10^{-7} As$_4$	19.89	1.14
20	Ge(As)	325	11	10^{-7} As$_4$	19.85	1.10
21	Ge(As)	325	9	10^{-6} As$_4$	19.96	1.21
22	Ge(P)	250	11	10^{-6} P$_2$	19.87	1.12
23	Si(As)	250	14	10^{-7} As$_4$	19.98	1.23

[a] Substrate cleaned in 10^{-6} Torr As$_4$.
[b] Substrate cleaned in 10^{-7} Torr As$_4$.

sity associated with As-doped, molecular-beam epitaxy (MBE)-grown Ge films on GaAs (100) has been studied[25,26] as a function of substrate temperature and found to vary relatively slowly in this temperature range. This behavior may be related to the relatively small variation of E'_F with substrate temperature observed in Fig. 3(b), where there is a tendency for E'_F to increase with increasing substrate temperature and with increasing As$_4$ background pressure during Ge deposition. The observed E'_F values are in the same range as those previously observed for n-Ge layers grown on several GaAs (100) surfaces,[9] and support the conclusion that As doping of Ge is important in determining E'_F while deposition-induced defects are not.[27]

To investigate the role of As in determining E'_F, two additional experiments were performed in an effort to separate the effect of As at the Ge/GaAs interface from As incorporated in the Ge overlayer. The results of these two experiments are shown in Fig. 3(c). In this case, the sample has two overlayers. The first layer was Ge deposited in vacuum at 250 °C; the E'_F value associated with this layer is shown by the open circles. The second Ge(As) overlayer was deposited at 250 °C in the presence of 10^{-7} Torr As$_4$ background

pressure. The E'_F observed after deposition of the Ge(As) layer is shown by closed circles. The large increase in the E'_F position (decrease in GaAs band bending) is indicated by arrows in Fig. 3(c). In Fig. 3(a), it was observed that exposure of a vacuum-deposited Ge layer to As$_4$ caused only a minor shift of E'_F. Taken together with the results shown in Fig. 3(c), it appears that the role of As is to alter the E_F in the deposited Ge and thus the Ge/GaAs E'_F rather than directly affecting the interface properties per se.

If As acting as a donor in Ge is responsible for the large E'_F values, other n-type dopants might be expected to produce a similar effect. Thus, a Ge(P) overlayer was prepared by depositing Ge at 250 °C in a 10^{-6} Torr P$_2$ background pressure. The measured E'_F value is shown in Fig. 3(d) and is similar to the results obtained with Ge(As) layers.

The above noted range in E'_F indicates that interface heterojunction band alignment characteristics may be responsible for the limits to the large range of observed E'_F values at the Ge/GaAs interface. To investigate this possibility, an overlayer of Si(As) was deposited at 250 °C in 10^{-7} Torr As$_4$ background pressure. The E'_F measurement is noted in Fig. 3(e) and indicates very small GaAs band bending.
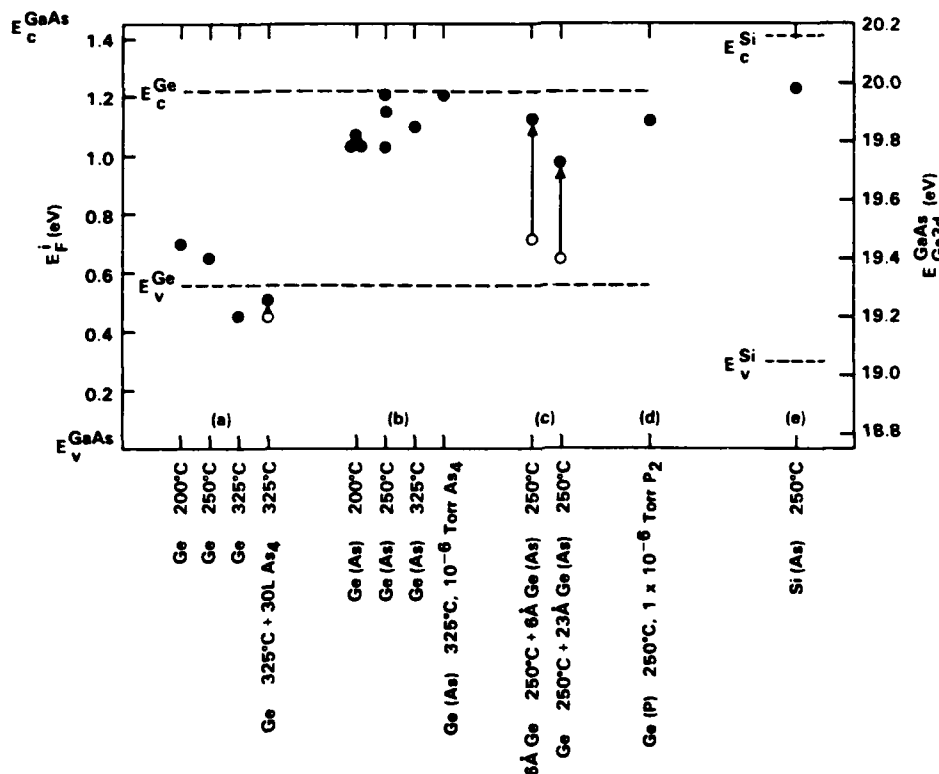
FIG. 3. Summary of several E_F^i measurements. Overlayer characteristics are given at bottom of figure. Unless noted otherwise, overlayer thicknesses are nominally ~10 Å and depositions intended to incorporate As or P in the overlayer were carried out in 10^{-7} Torr background pressure of As_4 or P_2: (a) Ge overlayers deposited in vacuum; (b) Ge overlayers deposited in As_4; (c) Ge overlayers initially deposited in vacuum, but completed with deposition in As_4; (d) Ge overlayer deposited in P_2; (e) Si overlayer deposited in As_4.

The above noted range in E_F^i indicates that interface heterojunction band alignment characteristics may be responsible for the limits to the large range of observed E_F^i values at the Ge/GaAs interface. To investigate this possibility, an overlayer of Si(As) was deposited at 250 °C in 10^{-7} Torr As_4 background pressure. The E_F^i measurement is noted in Fig. 3(e) and indicates very small GaAs band bending.

V. CONCLUSIONS

The widely varying values of E_F^i that have been observed for the Ge/GaAs interface, both in this work and in many previously published works[5,8,9,17,24,27,28] appear to be approximately confined to within the Ge band gap, as noted in Fig. 3. A very plausible explanation for this limit to the E_F^i values is that E_F^i depends on the net donor or acceptor density in the Ge. This model suggests that E_F^i is not necessarily pinned at the Ge/GaAs interface, but rather is restricted in total movement by the large density of states in the valence and conduction bands of Ge at the heterojunction interface.

The fact that the interface heterojunction characteristics seem important in determining the E_F^i value is supported by noting that both Ge(As) and Si(As) overlayers can produce very large E_F^i values. Also, it is well known that two-dimensional electron and hole gases can be observed at the technologically important AlAs/GaAs interface so that in this case

E_F^i in GaAs can be moved across the entire GaAs band gap. It appears therefore that even very thin (~10 Å) semiconductor heterojunction interfaces can overcome or remove the dominant E_F pinning mechanism observed at most GaAs interfaces. The formation of a heterojunction interface can be expected to remove dangling bond states that may otherwise contribute to pinning at the interface. Alternatively, a heterojunction interface might remove defects associated with pinning or overcome their influence by a charge transfer between carriers in the overlayer and these defects.

Is it well-known that ρ_c for alloyed AuGe based contacts depends sensitively on annealing conditions. In some investigations of alloyed AuGe contacts,[29] epitaxial regions of Ge have been observed in contact with the GaAs. It seems possible that E_F^i variations associated with the changing size, thickness and doping of thin epitaxial Ge regions could be affecting ρ_c during alloying. Because ρ_c for a tunneling contact depends exponentially on ϕ_B, the realization of a stable high E_F^i GaAs interface could have an important application in nonalloyed ohmic contact design.

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Metal contacts to GaAs with 1 eV Schottky barrier height

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Metal Schottky barrier contacts to n-type (100) GaAs are described in which a 1 eV Schottky barrier height ϕ_B is achieved by using a very thin Si interface layer to influence the interface Fermi energy E'_F. The metals investigated are Au, Cr, and Ti. The contact structure consists of a thick metal in combination with a ~ 15–30 Å heavily p-type Si interface layer. The E'_F and interface composition during initial contact formation were obtained by x-ray photoemission spectroscopy (XPS); the ϕ_B for the corresponding thick contacts was measured by current-voltage (I-V) and capacitance-voltage (C-V) techniques. The XPS, I-V, and C-V measurements gave consistent results. The 1 eV ϕ_B for the Si interface layer contact structure is independent of the contact metal.

The metal contacts to GaAs commonly used in device applications generally exhibit a restricted range of Schottky barrier height ϕ_B that is between ~ 0.7 and 0.9 eV. The performance of many GaAs device designs which include Schottky barrier contacts is improved, however, if a larger ϕ_B contact can be employed. Some unconventional Schottky barrier contacts where ϕ_B is ~ 1 eV have been reported; for example, polymeric $(SN)_x$,[1] amorphous Si-Ge-B material,[2] and Au with interface chalcogen.[3] Thus, an upper limit for ϕ_B established for ideal metal contacts[4] (no interface oxide) is not an intrinsic property of all GaAs Schottky barrier interfaces.

This letter reports 1 eV ϕ_B metal Schottky barrier contacts to GaAs in which the barrier increase is accomplished by influencing the interface Fermi energy E'_F with a very thin Si interlayer. The metals investigated are Au, Cr, and Ti. The contact structure consists of a thick metal and a ~ 15–30 Å Si interface layer made heavily p type with Ga. During initial contact formation E'_F and interface composition were observed by x-ray photoemission spectroscopy (XPS). For thick contacts, ϕ_B was measured by current-voltage (I-V) and capacitance-voltage (C-V) techniques on the same interfaces characterized by XPS. The XPS, I-V, and C-V measurements gave consistent results.

The contacts were prepared in the ultrahigh vacuum environment (10^{-10} Torr range base pressure) of an XPS apparatus that consists of a HP5950 electron spectrometer ($h\nu = 1486.6$ eV monochromatic x-ray source, ~ 16 Å effective photoelectron escape depth) and a custom sample preparation chamber. XPS spectra of the As $3d$, Ga $3d$, and of other appropriate core levels were obtained at different stages of initial contact interface formation. Electrical measurements were made with a computerized system that includes a HP4140B pA meter/voltage source and a HP4275A capacitance meter.

The GaAs used was (100) Bridgman-grown n-type ($\sim 5 \times 10^{16}$ cm^{-3} Si) wafers. To prepare a sample, a $\sim 8 \times 8$ mm GaAs piece is etched in fresh 4:1:1 H_2SO_4:H_2O_2:H_2O solution for ~ 30 s to remove polishing damage, mounted on a Mo plate with In, and immediately put into the XPS system. The native oxide is removed from the GaAs surface by momentary heating to the minimum necessary temperature (~ 575 °C). This thermally cleaned surface is free of O

and C (as shown by XPS), and is ordered (exhibits a characteristic low-energy electron diffraction pattern). The Si layer evaporation source was a Ta basket filled with heavily p-type (B) Si. The Ga evaporation source was a miniature W basket located near the sample. Au, Cr, and Ti contact metals were evaporated from W baskets. After XPS analysis of an initial thin metal overlayer (~ 10–15 Å), a final thick metal layer of > 2000 Å was deposited. An array of circular 2.54×10^{-2} cm diameter contacts was defined by photolithography and etching. The electrical measurements were thus taken on the same interfaces characterized by XPS.

The Si interface layers, which ranged from 17 to 28 Å, were deposited at ~ 0.1 Å/s onto clean GaAs surfaces held at 250 °C (the layer thickness was measured by noting the attenuation of the As $3d$ peak from the GaAs substrate). Low E'_F (large ϕ_B) results were obtained most consistently when both a monolayer of Ga was deposited during the first few seconds of the Si overlayer growth and the chamber was backfilled with $\sim 2 \times 10^{-6}$ Torr H_2. This amount of Ga is in excess of what can be incorporated into Si films in the thickness range used, thus ensuring that sufficient p-type dopant is available to produce degeneracy. The resultant Si layer is designated Si(Ga). The hydrogen background seems to assist in making the Si films p type. Although we surmise that hydrogen helps by minimizing the amount of electrically active deep levels in the Si, the exact mechanism(s) involved is not clear. Other Si deposition conditions also yielded low E'_F interfaces, as will be briefly discussed later.

The As $3d$ data in Fig. 1 illustrate how XPS was used to measure E'_F (and ϕ_B) during contact interface formation (other details on the XPS technique can be found elsewhere[5]). The top three peaks are for sequential treatments to the same sample; the bottom peak is for the indicated two overlayers (peak heights are normalized). The inset in Fig. 1 depicts the relationship between the As $3d$ core level in GaAs at the interface and E'_F (the photoelectron escape depth is much smaller than the band bending depth). Thus, $E'_F = E_{As\,3d} - 40.74$ eV, where $(E_{As\,3d} - E_v) = 40.74 \pm 0.03$ eV is the constant As $3d$ to valence-band maximum energy difference in GaAs[6] (note that the XPS binding energy E_B scale is zero at the sample Fermi energy). The vertical line indicating the center (midpoint of the width at half-maximum) of the clean surface As $3d$ peak at 41.58 eV
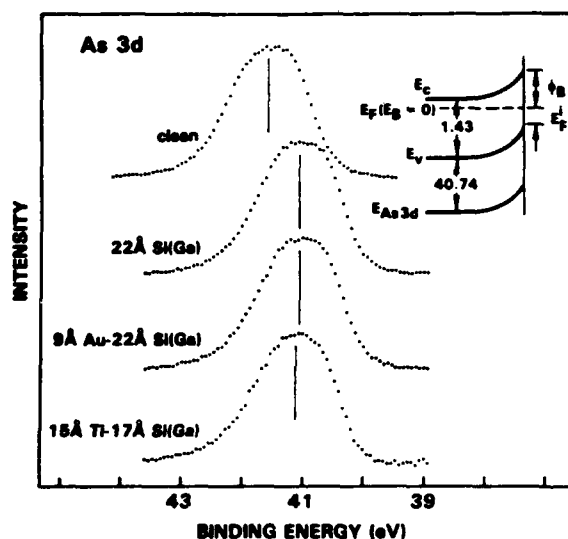
FIG. 1. XPS As $3d$ core level spectra for various thin overlayers on clean n-type GaAs (100) surfaces. Inset shows relationship between As $3d$ binding energy and E'_F.
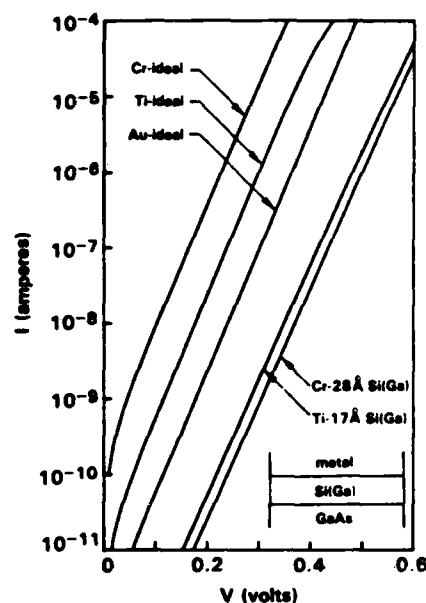

FIG. 2. Representative I-V data for Cr-Si(Ga) and Ti-Si(Ga) contacts compared to corresponding ideal contacts [Au-Si(Ga) data not shown because of overlap with Cr-Si(Ga) data]. Contact area = 5.07×10^{-4} cm^2.

therefore gives an E'_F (clean) measurement of 0.84 eV (the average value for four samples was 0.79 eV).

Deposition of 22 Å of Si(Ga) onto the clean GaAs surface caused a 0.51 eV decrease of the As $3d$ binding energy to 41.07 eV, which gives $E'_F = 0.33$ eV (compare upper two peaks in Fig. 1). Similar E'_F data for the other samples are listed in Table I. Each sample has a low (0.33–0.47 eV) E'_F value after deposition of a Si(Ga) overlayer.

Is the low E'_F value at the Si(Ga)-GaAs interface retained after deposition of a contact metal? The third As $3d$ peak in Fig. 1 at 41.06 eV demonstrates that a 9 Å Au overlayer essentially did not change E'_F for the 22 Å Si(Ga) sample ($E'_F = 0.32$ eV). Similarly, the bottom As $3d$ peak at 41.12 eV ($E'_F = 0.38$ eV) is for a 15 Å Ti overlayer on the 17 Å Si(Ga)-GaAs interface. Thus, deposition of a metal does not increase the low E'_F value established by the Si(Ga) layer.

The E'_F measured with a metal overlayer is related to the Schottky barrier height (inset in Fig. 1) by $\phi_B = 1.43$

TABLE I. Schottky barrier height of metal contacts to GaAs that contain a thin Si(Ga) interface layer.

Contact	$E'_F{}^a$ (eV)	ϕ_B^{XPS} (eV)	n	$\phi_B^{IV\,b}$ (eV)	ϕ_B^{CV} (eV)
Au-22 Å Si(Ga)	0.33	1.11	1.08	1.01	1.01
Cr-28 Å Si(Ga)	0.41	···	1.11	0.99	1.10
Ti-17 Å Si(Ga)	0.39	1.05	1.11	0.98	1.14
Ti-26 Å Si(Ga)	0.47	1.01	1.10	0.97	1.06
Au-ideal			1.05	0.89	
Cr-ideal			1.05	0.76	
Ti-ideal			1.04	0.83	

^{a}Si(Ga) overlayer only.
^{b}Includes + 0.04 eV image force correction.

eV $- E'_F$. The values of ϕ_B^{XPS} for the Au and Ti samples are given in Table I [the Cr ϕ_B^{XPS} could not be measured because the As $3d$ and Cr $3p$ peaks overlap and there was an additional 0.05 eV decrease in E'_F at the 26 Å Si(Ga)-GaAs interface upon Ti deposition]. Thus, XPS measurements show that thin metal contacts to Si(Ga)-GaAs interfaces have ~1 eV Schottky barrier heights.

Representative I-V data for the thick metal Cr-28 Å Si(Ga) and Ti-17 Å Si(Ga) contacts are plotted in Fig. 2 [the Au-22 Å Si(Ga) data are not shown because of overlap with the Cr-Si(Ga) data]. For comparison, I-V data for ideal contacts of these metals (metal deposited onto clean GaAs surface) are also shown. A substantial increase in barrier height is evident for the contacts with the Si(Ga) interlayer. The I-V data were analyzed with respect to the thermionic emission model[7] for current transport:

$$I = I_S \exp(qV/nkT)[1 - \exp(-qV/kT)]A,$$

where the ideality factor $n(\sim 1.02$ is ideal) and I_S were determined by a least-squares fit. The Schottky barrier height ϕ_B^{IV} is related to I_S by $I_S = SA^*T^2$ $\times\exp[-q(\phi_B^{IV} - \Delta\phi)/kT]A$, where S is the contact area, $A^* = 8.16$ is the effective Richardson constant, and $\Delta\phi = 0.04$ eV is the calculated image force correction. The corresponding C-V data for each contact, taken at 1 MHz over a $+0.2$ to -2.0 V range, were analyzed according to the conventional model[8] that gives ϕ_B^{CV} in terms of the intercept V_i (found by a least-squares fit) on the voltage axis of a $1/C^2$ vs V plot. There were no significant deviations from linearity in these $1/C^2$ vs V plots. Table I lists the average values of n, ϕ_B^{IV}, and ϕ_B^{CV} for each metal-Si(Ga) sample (~10 contacts per sample, $< \pm 0.01$ eV estimated measurement uncertainty). The ϕ_B^{IV} for the corresponding ideal contact is also given.

The electrical measurements on the thick contacts confirm the 1.0 eV barriers measured by XPS. Why ϕ_B^{CV} is ~0.1 eV larger than ϕ_B^{IV} for the Cr-Si(Ga) and Ti-Si(Ga) contacts is unexplained but is most likely an artifact of the C-V model used; the close agreement of the values for the Au-Si(Ga) contact shows this difference is not an intrinsic feature of the metal-Si(Ga)-GaAs interface. For this reason the ϕ_B^{IV} values will be considered the most accurate measure of the barrier height. The ideality factors are acceptably low. The increased ϕ_B for the metal-Si(Ga) contact compared to the respective ideal contact ranges from 0.1 eV (Au) to 0.23 eV (Cr). In addition, the metal-Si(Ga) ϕ_B is independent of the contact metal, which is in contrast with ideal contacts to GaAs.

The XPS results demonstrate that the large ϕ_B is caused by a low E'_F created at the Si(Ga)-GaAs interface which remains after deposition of a thick contact metal. This method of achieving a large barrier contact is thus distinct from methods[9] in which an effective barrier height is controlled by tailoring the impurity profile, and hence the potential, in the GaAs depletion region near a metal-GaAs interface where ϕ_B itself is fixed.

The critical factor for achieving a low E'_F at Si-GaAs interfaces is that the Si be heavily p type. In principle the Si layer should not be depleted. We have also produced low E'_F interfaces with boron-doped Si deposited at 200 and 350 °C in vacuum. Thus, neither the kind of p dopant nor the precise substrate temperature is a crucial parameter. The nonepitaxial nature of the Si and large lattice mismatch with GaAs also indicates that interface perfection need not be approached to obtain a low E'_F. Furthermore, a large E'_F = 1.23 eV value was recently reported[10] for the Si(As)-GaAs interface grown at 250 °C. Thus, E'_F is unpinned and can be varied up to ~0.9 eV at Si-GaAs interfaces by making the Si either p or n type. This observation suggests that the lower limit to E'_F values at Si-GaAs interfaces may be set by where the Si valence-band maximum falls within the GaAs band gap (that is, the Si-GaAs heterojunction valence-band offset ΔE_v). A ΔE_v of 0.23 ± 0.1 eV has

been measured,[11] which is fairly close to the E'_F values for the metal-Si(Ga)-GaAs contacts.

Our results offer a possible basis for understanding the high barrier measured for thick amorphous Si-Ge-B contacts[2] to GaAs. If heavily p-type material in intimate contact with the GaAs was produced by the chemical vapor deposition process that was used, then E'_F may have been unpinned in the same way as at the Si(Ga)-GaAs interfaces described here.

In summary, the ϕ_B of metal contacts to GaAs can be increased to 1.0 eV by inclusion of a very thin ~15-30 Å Si(Ga) interface layer to control E'_F. The metals investigated were Au, Cr, and Ti. The increased ϕ_B for these metals (compared to ideal contacts) ranges from 0.1 to 0.23 eV. Thus, use of the Si(Ga) interlayer also makes ϕ_B independent of the contact metal. Because of the diverse properties of Au, Cr, and Ti, we expect that other metals will also exhibit an increased ϕ_B when used in a similar metal-Si(p-type)-GaAs contact structure.

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Wide range of Schottky barrier height for metal contacts to GaAs controlled by Si interface layers

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Metal (Au, Cr, and Ti) contacts to n-type (100) GaAs are described in which the Schottky barrier height ϕ_B is controlled by using a very thin Si interface layer to influence the interface Fermi energy E'_F. The contact structure consists of a thick metal and an ~ 15–30 Å Si interface layer that is heavily either p-type or n-type. A large 1 eV ϕ_B is found for the metal–Si(p-type)–GaAs structure and a small 0.5 eV ϕ_B for the metal–Si(n-type)–GaAs structure. X-ray photoemission spectroscopy (XPS) was used to obtain E'_F and interface composition during initial contact formation; the ϕ_B for the thick contacts was measured by I–V and C–V techniques.

I. INTRODUCTION

Ideal metal contacts (no interface oxide) to n-type GaAs generally have a range in Schottky barrier height ϕ_B that is between ~ 0.7 and 0.9 eV.[1] However, this restricted ϕ_B range is not an intrinsic property associated with all GaAs contacts. For example, some unconventional large height Schottky barrier contacts where ϕ_B is ~ 1 eV are polymeric $(SN)_x$,[2] amorphous Si–Ge–B material,[3] and Au with interface chalcogen.[4] In contrast, low ϕ_B (<0.4 eV) contacts have also been reported, including Al with interface chalcogen[5,6] and Au contacts that have a thin (~ 10 Å) Ge interface layer.[7] Such an extended range in ϕ_B is of benefit in many GaAs device designs. Investigation of the conditions under which a wide range of ϕ_B can be attained at GaAs interfaces is thus of interest for both Schottky barrier contact and Ohmic contact device applications.

This paper reports metal (Au, Cr, and Ti) contacts to n-type GaAs in which ϕ_B is controlled over a wide range by influencing the interface Fermi energy E'_F with a very thin Si interface layer. The contact structure is a thick metal and an ~ 15–30 Å Si interface layer. For large ϕ_B contacts the Si is made heavily p-type with Ga or B. For small ϕ_B the Si is made heavily n-type with P. X-ray photoemission spectroscopy (XPS) was used to obtain interface composition and E'_F during initial contact formation. For thick contacts, electrical measurement of ϕ_B was by I–V and C–V techniques. The XPS, I–V, and C–V measurements gave consistent values for ϕ_B and E'_F.

II. EXPERIMENTAL

The thin Si–GaAs interfaces and subsequent thick metal contact layers were prepared within an XPS system that consists of a HP5950 electron spectrometer ($h\nu = 1486.6$ eV monochromatic Al $K\alpha$ x-ray source, ~ 16 Å effective photoelectron escape depth) and a custom ultrahigh vacuum (10^{-10} Torr range base pressure) sample preparation chamber. XPS spectra of the As $3d$, Ga $3d$, and other pertinent core levels were obtained at several stages of interface formation. Electrical measurements on thick contacts were made with a computerized system that includes a HP4140B

pA meter/voltage source and a HP4275A capacitance meter. I–V data were taken in 0.01 V forward bias increments to a current limit of 1 mA; C–V data were taken at 1 MHz in 0.1 V increments to a reverse bias of -2 V.

The GaAs used was (100) oriented bulk grown n-type ($\sim 5 \times 10^{16}$ cm^{-3}) wafers. Samples were prepared by etching an $\sim 8 \times 8$ mm GaAs piece in fresh 4:1:1 H_2SO_4:H_2O_2:H_2O solution for ~ 30 s to remove polishing damage, mounting it on a Mo plate with In, followed by immediate placement into the XPS system. A clean surface was obtained by momentary heating to the minimum temperature (~ 575 °C) required to remove the thin, ~ 10 Å, GaAs native oxide composed of Ga_2O_3 and As_2O_3. The resultant GaAs surface both is ordered [displays a characteristic low-energy electron diffraction (LEED) pattern] and is shown by XPS to be free of O and C. The Si source was an enclosed Ta wire basket. Si impurity dopant sources were a miniature W basket located near the sample for Ga, elemental B included in the Si source for B, and a piece of InP wrapped in resistively heated Ta wire for P. Au, Cr, and Ti contact metals were evaporated from W baskets. After XPS analysis of thin overlayer(s) a final thick metal overlayer of >2000 Å was deposited. Circular 2.54×10^{-2}-cm-diam contacts for electrical measurements were defined by photolithography and etching. Electrical measurements were thus obtained from the same interfaces that were characterized by XPS.

Si layers of ~ 10–30-Å thickness were deposited at ~ 0.1 Å/s onto clean GaAs surfaces held between 200 and 350 °C (measurement of layer thickness was by noting the attenuation of the As $3d$ peak from the underlying GaAs). For the B doped Si layers, designated Si(B), material from the Si source was evaporated in vacuum. The procedure for the Ga doped layers, Si(Ga), was somewhat more complex. The same Si source as for the Si(B) layers was used. Ga was introduced into the Si by depositing a monolayer of Ga during the first few seconds of Si growth. This amount of Ga is more than can be incorporated into the Si in the thickness range used, which ensures that sufficient Ga is available to produce degeneracy. The most consistent low E'_F Si(Ga)–GaAs interfaces were obtained when the chamber was back-

filled with $\sim 2 \times 10^{-6}$ Torr H_2 during the Si deposition. Evidently, the hydrogen assists in the p-type doping process by minimizing the number of electrically active deep levels in the Si, but the precise mechanism(s) involved is not obvious. Si layers with incorporated P, Si(P), were obtained by evaporation of lightly n-type (P) Si in an $\sim 2 \times 10^{-6}$ Torr P_2 background pressure.

Figure 1 illustrates how XPS is used to measure E'_F from the binding energy E_B of the As $3d$ core level peak *in GaAs* at an interface, designated $E_{As\,3d}$ (E_B is zero at the sample Fermi energy). The escape depth for As $3d$ photoelectrons is much smaller than the GaAs band bending depth. Thus referring to Fig. 1, $E'_F = E_{As\,3d} - 40.74$ eV, where $(E_{As\,3d} - E_v) = 40.74$ eV is the constant As $3d$ to valence band maximum binding energy difference in GaAs.[8] E'_F can be conveniently measured for overlayer(s) up to approximately twice the escape depth. If one of the overlayers is a metal, then $\phi_B^{XPS} = 1.43$ eV $- E'_F$.

I-V data were analyzed by using the thermionic emission model[9]: $I = I_S \exp(qV/nkT)[1 - \exp(-qV/kT)]$ A, where the ideality factor n (~ 1.02 is ideal) and I_S were determined by a least-squares fit. The Schottky barrier height ϕ_B^{IV} is related to I_S by $I_S = SA^*T^2 \exp[-q(\phi_B^{IV} - \Delta\phi)/kT]$ A, where S is the contact area, $A^* = 8.16$ is the effective Richardson constant, and $\Delta\phi$ is the calculated image force correction ($\Delta\phi = +0.04$ eV for $\phi_B \geqslant 0.7$ eV and $+0.03$ eV for $\phi_B < 0.7$ eV). C-V data were analyzed in terms of a conventional model[10] whereby ϕ_B^{CV} is related to the intercept V_i (which was found by a least-squares fit) on the voltage axis of a $1/C^2$ vs V plot. With the present GaAs material, $\phi_B^{CV} = V_i + 0.08$ eV. The estimated measurement uncertainty in ϕ_B^{IV} and ϕ_B^{CV} is $< \pm 0.01$ eV.

III. RESULTS

Figure 2 shows representative As $3d$ core level spectra to demonstrate the range in E'_F that results from Si(P), Si(B),
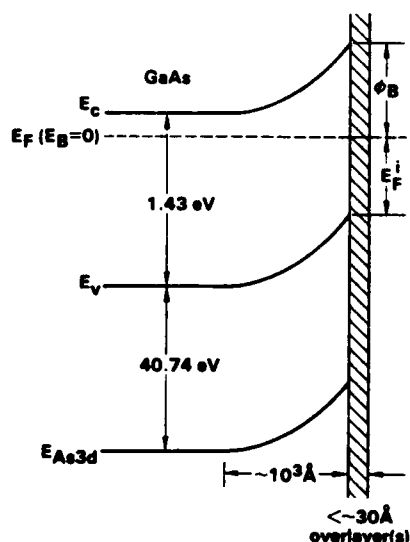

FIG. 2. XPS As $3d$ core level spectra for thin p-type and thin n-type Si layers deposited on clean n-type GaAs (100) surfaces.

FIG. 1. Schematic interface band diagram that illustrates the XPS measurement of E'_F and ϕ_B by using the As $3d$ core level in GaAs.

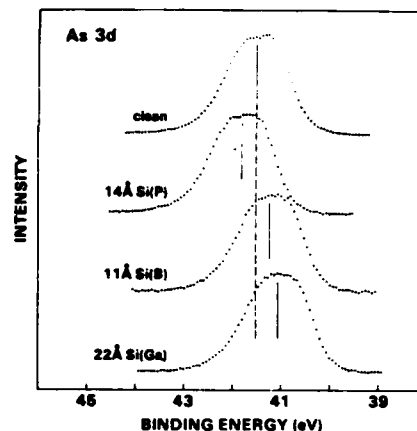and Si(Ga) overlayers deposited onto clean GaAs (100) surfaces (peak heights are normalized). The upper two peaks are for the same sample. Thus, the vertical line that indicates the center (midpoint of the width at half-maximum) of the clean surface As $3d$ peak at $E_{As\,3d} = 41.52$ eV corresponds to E'_F(clean) $= 0.78$ eV (the average value for 14 samples was 0.79 eV). Deposition of a 14 Å Si(P) overlayer onto this clean surface results in a 0.30 eV *increase* in binding energy to $E_{As\,3d} = 41.82$ eV, which is a E'_F *increase* to $E'_F = 1.08$ eV. In contrast, overlayers of Si(B) (third peak, $E_{As\,3d} = 41.24$ eV) and Si(Ga) (bottom peak, $E_{As\,3d} = 41.07$ eV) have a *decrease* in E_B relative to the clean surface, which is thus a E'_F *decrease* to 0.50 and 0.33 eV, respectively. In this example, therefore, the range in E'_F at these Si-GaAs interfaces is 0.75 eV. Table I lists similar data for a number of samples in which thin Si(Ga), Si(B), and Si(P) overlayers were deposited onto clean GaAs surfaces. Also listed is a recently reported[11] value for E'_F at a Si(As)-GaAs (100) interface. The maximum range in E'_F for the Si-GaAs interfaces in Table I is 0.90 eV.

To make a Schottky barrier contact a metal is deposited onto the thin Si layers. Is the E'_F value established at the Si-GaAs interface affected by such metal deposition? To answer this question the value of E'_F (and thus ϕ_B, as discussed in Sec. II) after deposition of a thin (~ 10–20 Å) metal layer onto the Si layer was measured by XPS for some of the samples. Table II lists the ϕ_B^{XPS} measured for Au–Si(Ga), Ti–Si(Ga), and Au–Si(Γ) contacts (the Cr ϕ_B^{XPS} could not be measured because the As $3d$ and Cr $3p$ peaks overlap). Thus, for the thin metal–Si(Ga) contacts E'_F did not significantly change when a metal was deposited. There was, however, an ~ 0.1 eV decrease in E'_F for Au–Si(P). A large ~ 1-eV barrier is therefore predicted for thick contacts to Si(Ga)–GaAs and a small ~ 0.4-eV barrier for contacts to Si(P)–GaAs.

Representative I-V data for thick metal Au–22 Å Si(Ga), Cr–24 Å Si(B), and Au–25 Å Si(P) contacts are plotted in Fig. 3. Also shown for comparison are data for ideal contacts of these metals (metal deposited onto a clean GaAs surface).

TABLE I. Interface Fermi energy E'_F after deposition of various thin Si layers which contain n-type or p-type impurities onto clean n-type GaAs(100) surfaces.

Impurity	Si thickness[a] (Å)	$E_{As\ 3d}$[b] (eV)	E'_F (eV)
Ga	17	41.13	0.39
Ga	22	41.07	0.33
Ga	26	41.21	0.47
Ga	28	41.15	0.41
B	11[c]	41.24	0.50
B	24[c]	41.28	0.54
B	25[d]	41.23	0.49
P	14	41.82	1.08
P	25	41.84	1.10
As[e]	14		1.23

[a] Except as noted, Si deposited at 250 °C.
[b] As $3d$ binding energy in GaAs with Si overlayer.
[c] 200 °C.
[d] 350 °C.
[e] Reference 11.

FIG. 3. Representative I–V data for Au–Si(Ga), Cr–Si(B), and Au–Si(P) contacts compared to Au-ideal and Cr-ideal contacts (contact area = 5.07×10^{-4} cm^2).

A significant increase in barrier height is apparent for Si(Ga) and Si(B) interlayer contacts as is a significant decrease for the Si(P) contact. Table II gives the average n and ϕ_B^{IV} measured for each Si interlayer contact sample (also given is the ϕ_B^{IV} for the corresponding ideal metal contact).
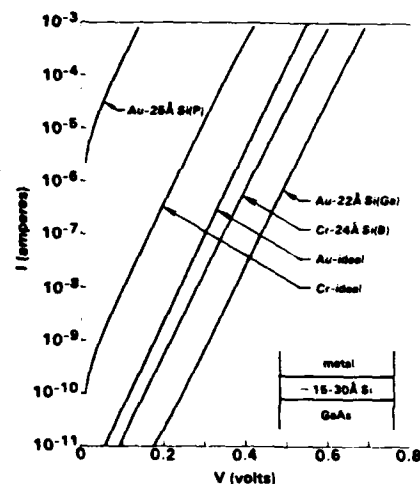
Representative C–V data for the Au–Si(Ga), Au–Si(P), and Au–ideal contacts are shown in the $1/C^2$ vs V plots of Fig. 4. The C–V data for the other contact samples were similar in form. The average ϕ_B^{CV} measured for each sample is listed in Table II.

IV. DISCUSSION

The I–V and C–V electrical measurements of ϕ_B on thick contacts are consistent with the E'_F (ϕ_B) values measured by XPS with thin overlayers. Why ϕ_B^{CV} is ~0.1 eV > ϕ_B^{IV} for the Cr and Ti contacts with Si(Ga) and Si(B) interlayers and an opposite sign difference of 0.07 eV is measured for the Au–Si(P) contact is not clear. The agreement between I–V
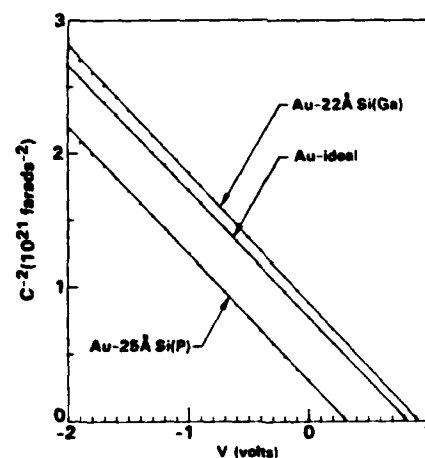
and C–V values for the Au–Si(Ga) contact, however, indicates that such disparities are not an intrinsic characteristic of all metal–Si–GaAs contacts. Since the discrepancies are comparatively minor and may be an artifact of the C–V model, for discussion purposes the I–V values will be used: for the thick Si(Ga) contacts $\phi_B = 1.0$ eV; for the Cr–Si(B) contact $\phi_B = 0.92$ eV; and for the Au–Si(P) contact $\phi_B = 0.5$ eV. The I–V ideality factors are acceptably small. Compared to the respective ideal contacts, the ϕ_B increase ranges from 0.1 eV (Au) to 0.23 eV (Cr) while the ϕ_B decrease for Au is 0.4 eV. By use of the metal–Si(p-type)–GaAs structure ϕ_B can be made essentially independent of the contact metal.

The XPS measurements show that the wide range in ϕ_B for these metal–Si contacts is a direct consequence of the wide range in E'_F that can be induced at the Si–GaAs interface. This mechanism for achieving a wide range in ϕ_B is thus quite unlike methods[12] in which a variable effective barrier height is created by tailoring the impurity profile, and therefore the potential, in the GaAs depletion region adjacent to a

TABLE II. Schottky barrier height ϕ_B of metal contacts to GaAs that include a thin Si interface layer.

Contact	ϕ_B^{XPS} (eV)	n	ϕ_B^{IV}[a] (eV)	ϕ_B^{CV} (eV)
Au–22 Å Si(Ga)	1.11	1.08	1.01	1.01
Cr–28 Å Si(Ga)	···	1.11	0.99	1.10
Ti–17 Å Si(Ga)	1.05	1.11	0.98	1.14
Ti–26 Å Si(Ga)	1.01	1.10	0.97	1.06
Cr–24 Å Si(B)	···	1.09	0.92	0.97
Au–14 Å Si(P)	0.43	1.05	0.53	0.46
Au–25 Å Si(P)	0.42	1.06	0.49	0.42
Au-ideal		1.05	0.89	
Cr-ideal		1.05	0.76	
Ti-ideal		1.04	0.83	

[a] Includes image force correction, see the text.

FIG. 4. Representative C–V data for Au–Si(Ga), Au–Si(P), and Au-ideal contacts. Line is least squares fit extrapolation to V_r.

metal–GaAs interface where ϕ_B itself remains constant.

Low E_F^i (high ϕ_B) values have been obtained both with Ga and with B heavily doped Si layers and high E_F^i (low ϕ_B) values both with P and with As heavily doped layers (in principle the Si layer should be degenerate and undepleted). Deposition temperatures between 200 and 350 °C were used. A LEED pattern was observed for the 350 °C growth which indicated epitaxy, but the lower temperature growths were either amorphous or polycrystalline. Thus, neither a precise Si growth temperature (although the lower and upper limits have not been determined) nor a particular Si impurity are crucial. The large lattice mismatch of Si and GaAs and the generally nonepitaxial nature of the Si layers also show that the degree of Si–GaAs interface perfection is unimportant. The essential condition influencing E_F^i at the Si–GaAs interface is that the Si be heavily either n-type or p-type.

Some difficulty was encountered in growing sufficiently heavy p-type Si films. The results with the B dopant were erratic with the method employed and there were some samples where the Si–GaAs E_F^i was not low because the Si apparently failed to be heavily p-type. Although lower E_F^i values were obtained with Ga, this should not be considered an inherent limitation of using B as a dopant but rather a requirement for good control over the Si dopant incorporation process. In this respect, the procedure for the Ga doped films yielded better consistency in producing low E_F^i interfaces, although the importance of the hydrogen background needs to be clarified. On the other hand, heavily n-type Si by P incorporation was readily obtained. Under the conditions used the Si layer had a large P excess detected by XPS; the amount of P can probably be controlled by changing the level of P overpressure or the substrate temperature.

A E_F^i range of ~0.7 eV at thin Ge–GaAs interfaces [n-type (100) GaAs] that results from making the Ge heavily either n-type or p-type has been reported.[7,11] This range is similar to the 0.66 eV band gap of Ge and consistent with the Ge–GaAs band lineup, which thus strongly suggests that the Ge band gap magnitude is what determines the extent to which E_F^i can be varied at this interface. In Table I the maximum E_F^i unpinned range for thin Si–GaAs interfaces is ~0.7 eV for the present data [~0.8 eV if the previously reported Si(As)–GaAs interface is included]. By analogy with the Ge–GaAs interface, an E_F^i range of ~1.1 eV is predicted at the Si–GaAs interface based on the 1.12 eV crystalline Si band gap. It is reasonable to expect that the value of E_F^i at its lower limit will be approximately set by where the Si valence band maximum lies within the GaAs band gap, which is the Si–GaAs heterojunction valence band offset ΔE_v. A ΔE_v of 0.23 ± 0.1 eV has been measured[13] for the Si–GaAs interface, a value less than but in fair accord with the Si(Ga)–GaAs E_F^i results. Thus, an additional decrease in E_F^i at Si(p-type)–GaAs interfaces and an increase at Si-(n-type) interfaces amounting to ~0.3 eV in total (~0.4 for the Ga, B, and P dopants) is probable by refinement of the Si deposition process.

Unlike the comparatively constant E_F^i at Si(p-type)–GaAs interfaces with metal deposition, the Si(P)–GaAs E_F^i decreased ~0.1 eV with a Au overlayer. This effect may thus

occur for other metals. For many Ohmic contact applications the 0.5 eV ϕ_B obtained at the Au–Si(P)–GaAs contact may be sufficiently low. However, it is likely that the highest E_F^i at Si(n-type)–GaAs interfaces can be retained by interposing a thin layer of a nonmetal electrical conductor between the contact metal and the Si(n-type)–GaAs interface. This structure would thus be similar to that used for a GaAs nonalloyed Ohmic contact design[7] in which a high E_F^i at an ~10 Å Ge(As)–GaAs interface is maintained by such an interlayer (in one example NiAs$_x$ was used). If found necessary in some instances, the same principle of an electrically conducting isolation layer could also be applied to optimally maintain a low E_F^i at Si(p-type)–GaAs interfaces.

Like GaAs, other III–V compound semiconductors (InP, for example) tend to have a limited range of ϕ_B for metal contacts. If the mechanism that restricts ϕ_B in other III–V semiconductors is analogous to that for GaAs, the present results suggest that appropriately doped Si or Ge interlayers will also increase the ϕ_B range for metal contacts to such semiconductors.

V. SUMMARY

E_F^i values of 0.4 eV for Si(Ga), 0.5 eV for Si(B), and 1.1 eV for Si(P) are measured by XPS at Si–GaAs(100) interfaces, where the Si is an ~15–30-Å overlayer [a value of 1.2 eV has also been reported for Si(As)]. Thus, E_F^i at the Si–GaAs (100) interface is not pinned and can be moved over a wide 0.7–0.8-eV range by making the Si layer either p-type or n-type. For thick metal Au, Cr, and Ti contacts to the Si(Ga)–GaAs interface $\phi_B = 1.0$ eV; for Cr to Si(B)–GaAs $\phi_B = 0.92$ eV; and for Au to Si(P)–GaAs $\phi_B = 0.5$ eV. Inclusion of a thin ~15–30 Å heavily p-type or heavily n-type Si interface layer therefore allows the design of metal contacts to GaAs with an extended barrier height range compared to conventional metal contacts.

ACKNOWLEDGMENT

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Variations of GaAs (100) Interface Fermi Level
for Model AuGeNi Ohmic Contacts[*]

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The AuGeNi alloyed ohmic contact is widely used for n-GaAs. The heterogeneous nature of the alloyed metallization complicates analysis of the ohmic contact formation mechanism. It is usually assumed, however, that the interface Fermi level (E_F^i) position (relative to the valence band maximum) for the alloyed contact is $\sim$0.5-0.7eV (consistent with Schottky barrier (ϕ_B) heights observed for most metal contacts to n-GaAs) and that a large donor concentration associated with Ge indiffusion near the GaAs interface region during alloying produces a low resistance tunnel contact.

Model AuGeNi contacts to n-GaAs that involve layered structures have been investigated to correlate E_F^i with interface composition. The layers (prepared in ultra high vacuum) were fabricated from the Au, Ge, and Ni components used in the alloyed contact in addition to As and Te; these contacts were not alloyed in order to preserve interfaces of known composition. X-ray photoemission spectroscopy (XPS) and current-voltage (I-V) measurements were used to analyze the samples.

For very thin ($\sim$10Å) Ge epitaxial layers grown on n-GaAs under conditions where As was incorporated in the Ge [i.e., Ge(As)], an unusually large E_F^i = 1.0-1.2eV was observed by XPS; Ge grown in the same temperature range without As incorporation or deposited at room temperature yielded E_F^i = 0.4-0.7eV. Whether or not the large E_F^i(1.0 -1.2eV) associated with the $\sim$10Å Ge(As) layer could be retained depended on the composition of the next deposited layer. For example, deposition of thin $NiAs_x$ or Te onto the Ge(As) preserved the large E_F^i values (as determined by XPS), while deposition of thin Au or Ni layers shifted E_F^i from $\sim$1.1 to $\sim$0.7eV. I-V measurements of ϕ_B on these samples after making the overlayer thickness sufficient to fabricate contacts demonstrated that this E_F^i variation was preserved. Thus, $Au-NiAs_x-Ge(As)$ and Au-Te-Ge(As) contacts with high E_F^i ($\sim$1.0-1.2eV) have low ϕ_B ($\sim$0.25-0.4 eV) while Au-Ge(As) and Ni-Ge(As) contacts have ϕ_B 0.6-0.8eV. It is therefore possible to obtain the unusually large E_F^i values in thick contacts by an appropriate choice of layer structure.

The present results on model AuGeNi ohmic contacts suggest that microscopic nonuniform regions with low ϕ_B may be associated with alloyed AuGeNi ohmic contact formation. The unusually large E_F^i values observed may also provide a guide for the design of nonalloyed ohmic contacts.

Large Range of Interface Fermi Energy in n-GaAs (100) Induced by Thin Si Layers

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Clean surfaces of n-type GaAs (100) have interface Fermi energy E_F^i values (relative to the valence band maximum) near midgap . Several ways to significantly increase E_F^i with respect to these vacuum-clean surface values are known. For example, deposition of a ~15 Å Si layer with incorporated As results in an E_F^i of 1.23 eV.[1] We here report x-ray photoemission spectroscopy (XPS) interface data and electrical measurements on thick Schottky barrier contacts which show that thin (~15 Å) Si layers evaporated from a source containing B onto clean n-type GaAs (100) surfaces will cause a decrease in E_F^i to values as low as 0.43 eV. Thus, a large 0.8 eV range in E_F^i at Si-GaAs (100) interfaces can be induced via the dopant type in the thin Si overlayer. The ultimate E_F^i range at these interfaces appears to be limited by the magnitude of the Si bandgap. The Si-GaAs (100) results further demonstrate that E_F^i is not necessarily pinned within a narrow set of values at interfaces that involve n-type GaAs (100).

The samples were prepared in the UHV chamber of the XPS system. The Si overlayers were deposited onto thermally cleaned GaAs substrates that were at a temperature between 200 and 350°C. Although epitaxy was observed at 350°C the Si deposited at lower temperatures was not epitaxial. Thus, the Si-GaAs interface perfection was not a crucial factor for achievement of a low E_F^i value. The E_F^i during interface formation was measured by analysis of XPS core level peaks. Schottky barrier contacts for electrical characterization were formed by depositing a thick layer of metallization onto the ~15 Å Si overlayer. For chromium and conducting chromium phosphide contacts the low E_F^i values at the Si-GaAs interface were retained and barrier heights of ~1 eV were measured by I-V and C-V techniques consistent with the associated XPS measurements. The corresponding Schottky barrier heights for ideal (no Si interlayer) contacts of these metallizations are ~0.2 eV lower. Thus, use of a thin p-type Si interlayer at n-GaAs (100) Schottky barrier contacts is a method to considerably increase barrier height compared to that generally obtained with ideal metal contacts.

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EFFECT OF Si AND Ge INTERFACE LAYERS ON THE SCHOTTKY
BARRIER HEIGHT OF METAL CONTACTS TO GaAs. J. R.
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Conventional metal contacts to GaAs generally have a
relatively narrow Schottky barrier height ϕ_B range of
~0.7-0.9 eV for n-type material and ~0.5-0.6 eV for
p-type. We describe recent results in which it has
been found that the metal contact ϕ_B range for both
n-type and p-type GaAs can be significantly extended
by inclusion of very thin Si or Ge interlayers that
directly influence the interface Fermi energy E_F^i.
X-ray photoemission spectroscopy was used to obtain
E_F^i and composition during contact formation; the ϕ_B
for the corresponding thick contacts was measured by
electrical methods. The Si and Ge interlayers are
~15-30 Å thick and are heavily either n type or p
type. In an appropriate structure, the ϕ_B range for
contacts to n-type GaAs can be as large as ~0.25 to
1 eV. For p-type GaAs, ϕ_B values of ~0.7-0.9 eV have
been obtained. The results will be discussed in
terms of a simple heterojunction model of the
interlayer-GaAs interface.

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DISCLOSURE
OF
INNOVATION OR INVENTION

Title Design of Nonalloyed Ohmic Contacts with Low Barrier Heights   Docket No. __87SC36__

INNOVATOR OR INVENTOR	DEPT. NO. & MAIL ADDRESS		SERIAL NO.	SOC. SEC. NO.	PHONE NO.	SUPERVISOR
J.R. Waldrop	311	A16		557-60-0219	4249	R.W. Grant
R.W. Grant	311	A16		276-34-1884	4219	C.A. Liechti

THE PROBLEM: __Reduction of barrier height at semiconductor interfaces for nonalloyed__
__tunneling ohmic contact applications.__

DESCRIPTION OF SOLUTION: (Succinct statement of broad solution together with detailed description, illustrated by sketches where appropriate, of the structure, operation, physical characteristics — — electrical, chemical, mechanical — — describing the new result. Attach additional material, preferably on Form 74-S.)

Nonalloyed ohmic contacts to GaAs and other semiconductors are increasingly important as device dimensions decrease. Many semiconductors (including GaAs) exhibit a narrow range of Fermi level positions at the interfaces of electrical contacts. This range is typically not optimum for nonalloyed tunneling ohmic contact applications because the specific contact resistance depends exponentially on barrier height. Gallium Arsenide is a semiconductor where the Schottky barrier height on n-type material is usually limited to a narrow range (0.7 to 0.9 eV) for metal contacts. This large barrier is thus an impediment to achieving a low ohmic contact resistance. A solution to the problem is to deposit very thin layers (on the order of 10Å) of another heavily doped semiconductor onto the semiconductor being considered. For n-GaAs it is observed that heavily n-type doped Ge or Si can lower the Schottky barrier height to ~0.25 - 0.4 eV. By use of a suitable nonmetallic conducting diffusion barrier, this low Schottky barrier height can be retained for metal contacts of thickness (>2000Å) that are suitable for practical applications. (The low barrier is not retained if the contact metal is directly against the thin semiconductor overlayer.) The role of the diffusion barrier is thus to isolate the semiconductor interface from the metal contact material while also providing a conducting electrical contact. The intermediate conducting layer does not itself introduce any electrical potential barrier. The thin heavily doped semiconductor layer either removes or overcomes the mechanism responsible for the normally observed narrow range of interface Fermi level positions but is thin enough so as not to introduce significant series resistance.

DISCLOSURE
OF
INNOVATION OR INVENTION

Title Method for Obtaining Metal Contacts with Large Schottky Barrier Heights   Docket No. __88SC46__

INNOVATOR OR INVENTOR	DEPT. NO. & MAIL ADDRESS	SERIAL NO.	SOC. SEC. NO.	PHONE NO.	SUPERVISOR
J.R. Waldrop	312 A4		557-60-0219	4249	P.M. Asbeck
R.W. Grant	315 A16		276-34-1884	4219	D.T. Cheung

THE PROBLEM: __Conventional metal Schottky barrier contacts to compound semiconductors__
__have limited range of barrier height.__

DESCRIPTION OF SOLUTION: (Succinct statement of broad solution together with detailed description, illustrated by sketches where appropriate, of the structure, operation, physical characteristics – – electrical, chemical, mechanical – – describing the new result. Attach additional material, preferably on Form 74-S.)

Metal contacts to n-type GaAs commonly used in device applications generally have a limited range of Schottky barrier height that is ~0.7 and 0.9 eV; the actual barrier height value within this range depends on the metal involved. It would be advantageous for certain device applications both to increase the contact barrier height over that customarily obtainable and to make the height independent of the contact metal. Both these objectives can be accomplished by using a contact formation method that is based on influencing the barrier height with a very thin (~15 – 30Å), heavily p-type, Si interlayer. This Si interlayer serves to overcome (compensate) the mechanism(s) at the metal-GaAs interface which would otherwise fix the barrier height (interface Fermi energy) for a particular metal at a lower value. It has been found that Si doped with either Ga or B will produce the desired effect of increasing the barrier. For Au, Cr, and Ti contacts with such a Si interlayer heavily doped with Ga the barrier height is 1 eV, independent of the metal. The increased barrier for these metals compared to the corresponding ideal (no interlayer) contact ranges from 0.1 to 0.23 eV. Because of the diverse properties of Au, Cr, and Ti it is expected that other metals will also have an increased barrier when used in the metal-Si(p-type)-GaAs contact structure. It is further expected that for other compound semiconductors such as InP, a similar contact structure will also produce increased Schottky barrier heights.